1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,X1036

LAST_MODIFICATION=Thu Jul 12 17:54:35 2018

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0013100592	ENGINEERING RELEASED	2018-07-12

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DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Thu Jul 12 17:54:35 2018

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DRAWING TITLE: SCHEM,MLB,X1036

Apple Inc.

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Schematic / PCB /MCO #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-02424	1	SCHEM,MLB,X1036	SCH	CRITICAL	
820-00939	1	PCBF,MLB,X1036	PCB	CRITICAL	
056-04386	1	MCO,MLB,X1036	MCO	CRITICAL	

Module Parts

TBT X,T

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00356	2	IC,TBT,TITAN RIDGE,QTZZ,ES2,B0,CSP337	U2800,UB000	CRITICAL	TBT_TR:B0
338S00408	2	IC,TBT,TITAN RIDGE,QUJK,QS,C1,CSP337	U2800,UB000	CRITICAL	TBT_TR:C1_QS
338S00441	2	IC,TBT,TITAN RIDGE,QUJK,PRQ,C1,CSP337	U2800,UB000	CRITICAL	TBT_TR:C1

ACE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S01442	4	IC,CD3215,ACE,C0,USB PWR SW,BLNK,BGA96	U3100,U3200,UB300,UB400	CRITICAL	ACE:C0_nFBGA
353S01478	4	IC,CD3215,ACE2,USB PWR SW,BLNK,BGA123	U3100,U3200,UB300,UB400	CRITICAL	ACE2:A0
353S00961	4	IC,CD3215,ACE,C0,USB PWR SW,BLNK,jrBGA96	U3100,U3200,UB300,UB400	CRITICAL	ACE:C0

SOC PMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00342	1	IC,PMU,CALPE_L,D2249A0,OTP-AC,CSP324,0.5	U7800	CRITICAL	PMU:A0_C

SOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00386	1	POP.SOC,GIBRALTAR+1G 21NM,M,Dev,CSP1122	U3900	CRITICAL	SOC:1G_DEV
339S00388	1	POP.SOC,GIBRALTAR+1G 21NM,M,Dev,CSP1122	U3900	CRITICAL	SOC:2G_DEV

10Gb ETHERNET CONTROLLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00332	1	IC,ENET CONTROLLER,AQC107,B1,BGA224	U9600	CRITICAL	10G_ENET:B1

1Gb ETHERNET CONTROLLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0616	1	IC,ENET CONTROLLER,CAESAR,A0	U9300	CRITICAL	1G_ENET:A0

WiFi/BT CONTROLLER (Should have alternatives)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00458	1	IC,MODULE,HARPOON,ES7.7,LGA385	U3730	CRITICAL	WIFI:ES7

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00428	339S00458		ALL	IC,MODULE,WCF2/BT,HARPOON,USI,ES7.5,LGA385

HDMI CONTROLLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00347	1	PCON,MADEA,A4	UA800	CRITICAL	HDMI:A4

PoWER CONTROLLER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00928	1	IC,ISL95828A,IMVP0 CPU REG,QFN48,6x6mm	U7100	CRITICAL	

CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00457	1	CPU,CFL-H	U0500	CRITICAL	CPU:PES
337S00555	1	CPU,CFL-H,QQ5N,EQS,2.8GHz	U0500	CRITICAL	CPU_EQS:2.8G
337S00554	1	CPU,CFL-H,QQ5K,EQS,3.0GHz	U0500	CRITICAL	CPU_EQS:3.0G
337S00553	1	CPU,CFL-H,QQ5C,EQS,3.2GHz	U0500	CRITICAL	CPU_EQS:3.2G
998-12472	1	INTERPOSER,,CFL-H, BGA1440	U0500	CRITICAL	CPU:SOCKET
337S00570	1	CPU,CFL-H,SRCX4,PRQ,2.8GHz	U0500	CRITICAL	CPU:2.8G
337S00569	1	CPU,CFL-H,SRCX3,PRQ,3.0GHz	U0500	CRITICAL	CPU:3.0G
337S00568	1	CPU,CFL-H,SRCX2,PRQ,3.2GHz	U0500	CRITICAL	CPU:3.2G
337S00618	1	CPU,CFL-H,SRDEC,PRQ,3.6GHz	U0500	CRITICAL	CPU:3.6G

4C CPU

PCH

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00470	1	PCH-H,CNL,QNDQ,ES,A1,BGA874	U1200	CRITICAL	PCH:ES
337S00536	1	PCH-H,CNL,QNYJ,QS,B0,BGA874	U1200	CRITICAL	PCH:QS
337S00577	1	PCH-H,CNL,QNYJ,PRQ,B0,BGA874	U1200	CRITICAL	PCH:PRQ

SSD Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-12416	4	NAND,3DV3,42GBP,S4E,170G,T,SUB X,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:128_TB
998-12418	4	NAND,3DV3,85GBP,S4E,170G,T,SUB X,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:256_TB
998-12420	4	NAND,3DV3,128GBP,S4E,170G,T,SUBX,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:512_TB
998-12424	4	NAND,3DV3,256GBP,S4E,170G,T,SUBX,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:1T_TB
335S00323	4	NAND,3DV3,42GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:128_SD
335S00324	4	NAND,3DV3,85GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:256_SD
335S00325	4	NAND,3DV3,128GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:512_SD
335S00327	4	NAND,3DV3,256GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:1T_SD
335S00321	4	NAND,3DV4,256GB,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:1T_SM
335S00373	4	NAND,3DV4,512GB,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	SSD:2T_SM

<- new DVT

SSD ALTERNATIVES

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
998-12421	998-12420	ALL	SSD:512 TB W/X	SSD:512_TB

```
998-12416  SSD:128_TB_X or TB1
998-12417  SSD:128_TB_W or TB2          TB2 dropped per Marketing

998-12418  SSD:256_TB_X or TB1
998-12419  SSD:256_TB_W or TB2          TB2 dropped per Marketing

998-12420  SSD:512_TB_X or TB1
998-12421  SSD:512_TB_W or TB2

998-12424  SSD:1T_TB_X or TB1
998-12426  SSD:1T_TB_W or TB2           TB2 dropped per Marketing
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Apple Inc.

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Programmable Parts

TBT X ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	U2890	CRITICAL	TBT_X_ROM:BLANK
341S00987	1	IC,T29,TR0,V7.1,DEV,X1036	U2890	CRITICAL	TBT_X_ROM:POC
341S00987	1	IC,T29,TR0,V7.1,DEV,X1036	U2890	CRITICAL	TBT_X_ROM:PROTO
341S01094	1	IC,T29,TR0,V7.1,DEV,X1036	U2890	CRITICAL	TBT_X_ROM:PREEVT
341S01111	1	IC,T29,TBT-X,R1,V21.3,EXT,X1036	U2890	CRITICAL	TBT_X_ROM:EVT
341S01171	1	IC,T29,TBT-X,R1,V28.1,DXT,X1036	U2890	CRITICAL	TBT_X_ROM:DVT

TBT T ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	UB090	CRITICAL	TBT_T_ROM:BLANK
341S00988	1	IC,T29,TR1,V7.1,DEV,X1036	UB090	CRITICAL	TBT_T_ROM:POC
341S00988	1	IC,T29,TR1,V7.1,DEV,X1036	UB090	CRITICAL	TBT_T_ROM:PROTO
341S01095	1	IC,T29,TR1,V7.1,DEV,X1036	UB090	CRITICAL	TBT_T_ROM:PREEVT
341S01110	1	IC,T29,TBT-T,R0,V21.3,EVT,X1036	UB090	CRITICAL	TBT_T_ROM:EVT
341S01170	1	IC,T29,TBT-T,R0,V28.1,DVT,X1036	UB090	CRITICAL	TBT_T_ROM:DVT

MADEA(HDMI) SPI ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00049	1	MADEA SPI FLASH,8MB,1.8V,8P,USON	UA801	CRITICAL	HDMI_ROM:BLANK
341S00991	1	IC,HDMI(V1.106),DEV,X1036	UA801	CRITICAL	HDMI_ROM:PROTO
341S01096	1	IC,HDMI(V1.106),DEV,X1036	UA801	CRITICAL	HDMI_ROM:PREEVT
341S01112	1	IC,HDMI(V2.245),EVT,X1036	UA801	CRITICAL	HDMI_ROM:EVT
341S01172	1	IC,HDMI(V2.005),DVT,X1036	UA801	CRITICAL	HDMI_ROM:DVT

10G ETHERNET ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00269	1	IC SPI FLASH,32MBIT,3V,SOIC8	U9890	CRITICAL	10G_ENET_ROM:BLANK
341S00989	1	IC,ETHERNET 10GB (V2.9.15) DEV,X1036	U9890	CRITICAL	10G_ENET_ROM:PROTO
341S01045	1	IC,ETHERNET 10GB (V2.9.15) DEV,X1036	U9890	CRITICAL	10G_ENET_ROM:PREEVT
341S01113	1	IC,ETHERNET 10GB (V2.10.1) EVT,X1036	U9890	CRITICAL	10G_ENET_ROM:EVT
341S01173	1	IC,ETHERNET 10GB (V2.10.8) DVT,X1036	U9890	CRITICAL	10G_ENET_ROM:DVT

1G ETHERNET ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S1025	1	IC,SERIAL FLASH,2MBIT,2.7V,REV E,SOIC-8	U9390	CRITICAL	1G_ENET_ROM:BLANK
341S00990	1	IC,ETHERNET 1GB (V1.15) DEV,X1036	U9390	CRITICAL	1G_ENET_ROM:PROTO
341S01174	1	IC,ETHERNET 1GB (V1.15) DVT,X1036	U9390	CRITICAL	1G_ENET_ROM:DVT

BT SERIAL FLASH

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00256	1	IC,SPI SERIAL FLASH,2MBIT,1.8V,DFN8	U3750	CRITICAL	BT_FLASH:BLANK
341S00965	1	BT SFLASH ROM(V21) PROTO-2,X1036	U3750	CRITICAL	BT_FLASH:POC
341S01025	1	BT SFLASH ROM(V32) proto,X1036	U3750	CRITICAL	BT_FLASH:PROTO
341S01098	1	BT SFLASH ROM(V32) preEVT,X1036	U3750	CRITICAL	BT_FLASH:PREEVT
341S01119	1	IC,BT SFLASH ROM(V45),EVT,X1036	U3750	CRITICAL	BT_FLASH:EVT
341S01175	1	IC,BT SFLASH ROM(V56),DVT,X1036	U3750	CRITICAL	BT_FLASH:DVT

WLAN SERIAL EEPROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00214	1	IC,EEPROM,SER,UWIRE,16K,1.8V,DFN8	U3710	CRITICAL	WLAN_EEPROM:BLANK
341S00725	1	WIFI ROM,V01,WW1,X665	U3710	CRITICAL	WLAN_EEPROM:DVT

The same as proto and later

SOC ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00203	1	IC,FLASH,SPI,4MX8.1V8,DFN8	U4770	CRITICAL	SOC_ROM:BLANK

SEP EEPROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00469	1	IC,MCU,ARM,SC000,STLNX,A0,DIVKEY,DFN8	U4730	CRITICAL	SEPROM:LYNX
335S0888	1	IC,SERIAL I2C EEPROM,128KBIT,8P,MLP8	U4730	CRITICAL	SEPROM:OG

Alternatives section 1

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
152S00573	152S1778	ALL	INDUCTOR	
152S00748	152S00697	ALL	INDUCTOR	
152S00801	152S00695	ALL	INDUCTOR	
155S00363	155S00364	ALL	CMC	
353S00772	353S4070	ALL	DISPLAY MUX	
353S4068	353S4070	ALL	DISPLAY MUX	
376S00074	376S0855	ALL	DUAL FET	
372S0186	372S0185	ALL	TRANSISTOR	
371S00095	371S0567	ALL	DIODE	
371S0684	371S0495	ALL	DIODE	
371S00042	371S00125	ALL	DIODE	
339S00389	339S00388	ALL	H9ML	
311S00013	311S0508	ALL	BUFFER	
335S00270	335S00203	ALL	SoC ROM	
128S00081	128S0264	ALL	CAP	
128S0364	128S0264	ALL	CAP	
377S0155	377S0184	ALL	ESD Diode	
377S0077	377S0183	ALL	ESD Diode	
377S00079	377S00077	ALL	Diode	
377S0178	377S00031	ALL	ESD Diode	
376S00224	376S1128	ALL	FET	
353S01041	353S01042	ALL	Vref IC	
353S00750	353S00877	ALL	LDO	
376S0636	376S1004	ALL	FET	
311S0426	311S00007	ALL	BUFFER	
335S00213	335S0888	ALL	SEP ROM	
311S0596	311S0593	ALL	LOGIC GATE	
311S0372	311S0562	ALL	LOGIC GATE	
311S00138	311S0436	ALL	LEVEL SHIFTER	
311S0562	311S0372	ALL	LOGIC GATE	
311S00133	311S00130	ALL	BUFFER	
197S00118	197S00120	ALL	CRYSTAL	
197S0612	197S00120	ALL	CRYSTAL	
197S00053	197S00050	ALL	Y1900 radar 37073234	
197S00054	197S00050	ALL	Y1900 radar 37073234	
197S00055	197S00050	ALL	Y1900 radar 37073234	
197S00048	197S00036	ALL	Y3000,etc radar 37073152	
311S00121	311S0398	ALL	AND Gate DFN pack	
311S0398	311S00121	ALL	AND Gate DFN pack	
138S0860	138S0775	ALL	C7101,etc radar 38188751	
138S0933	138S0931	ALL	C7525,etc radar 38079576	

Alternatives section continued on CSA 142

PAGE TITLE
BOM Configuration

Apple Inc.

DRAWING NUMBER 051-02424
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Boss on TOP side

2x 860-00935.

B0400
8.70D4.2ID-1.75H-SM

B0401
8.70D4.2ID-1.75H-SM

9x 860-00913.

B0406
BOSS-3.00D1.20ID-2.80H-SM

B0409
BOSS-3.00D1.20ID-2.80H-SM

B0410
BOSS-3.00D1.20ID-2.80H-SM

B0412
BOSS-3.00D1.20ID-2.80H-SM

B0413
BOSS-3.00D1.20ID-2.80H-SM

B0414
BOSS-3.00D1.20ID-2.80H-SM

B0415
BOSS-3.00D1.20ID-2.80H-SM

B0417
BOSS-3.00D1.20ID-2.80H-SM

B0416
BOSS-3.00D1.20ID-2.80H-SM

Boss on BOTTOM side

2x 860-00929.

B0407
BOSS-6.00D5.95H-TH-1.4-2.6

B0418
BOSS-6.00D5.95H-TH-1.4-2.6

2x 860-1438.

B0404
4.00D1.55H-M1.6X0.35-ST

B0403
4.00D1.55H-M1.6X0.35-ST
WIFI

2x 860-01020.

B0419
BOSS-4.00D2.2ID-4.25H-SM

B0408
BOSS-4.00D2.2ID-4.25H-SM

CPU Sled on TOP side:

2x 806-16518

CKPLUS_WAIVE=TERMSHORTED
SP0400
SLED-CPU-X1035
SMT-PAD-SP

CKPLUS_WAIVE=TERMSHORTED
SP0401
SLED-CPU-X1035
SMT-PAD-SP

Antenna cable clips:

3x 806-15581.

CKPLUS_WAIVE=TERMSHORTED
CLIP-ANT-LONG-X1035
CL0400
SM

CKPLUS_WAIVE=TERMSHORTED
CLIP-ANT-LONG-X1035
CL0401
SM

CKPLUS_WAIVE=TERMSHORTED
CLIP-ANT-LONG-X1035
CL0402
SM

Shield Cans:

604-19182.DIMM Shield
SH0400
SM
SHLD-FENCE-DIMM-X1035

806-14422.H9ML Fence
SH0401
SM
SHLD-FENCE-GIB-X1035

806-14495.Harpoon Fence
SH0402
SM
SHLD-FENCE-HARPN-X1035

806-16657 HDMI Shield Can
SH0420
SM
SHLD-HDMI-X1035

806-14019.UBSC-IO EMI Fence
SH0404
SM
SHLD-FENCE-TOP-USBC-X1035

806-14020.IO EMI Fence
SH0407
SM
SHLD-FENCE-TOP-IO-X1035

806-14423.Ridge Shield
SH0405
SM
SHLD-FENCE-RIDGE-X1035

806-14022 SSD Fence
SH0406
SM
SHLD-FENCE-SSD-X1035

806-15424.Diplexer Shield Can
SH0408
SM
SHLD-MLB-DIPLEXERS-X1035

Through holes of shields:

DIMM shield holes:2x 998-13324

SL0411
TH-NSP
SL-1.5X0.55-1.9X0.95

SL0413
TH-NSP
SL-1.5X0.55-1.9X0.95

Harpoon shield holes:2x 998-04440

SL0400
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0401
TH-NSP
SL-1.2X0.4-1.5X0.7

USBC IO shield holes:2x 998-04440

SL0403
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0402
TH-NSP
SL-1.2X0.4-1.5X0.7

3-pack IO shield holes:1x 998-04440
1x 998-13325

SL0404
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0412
TH-NSP
SL-1.05X0.4-1.45X0.8

Ridges shield holes:2x 998-04440

SL0406
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0405
TH-NSP
SL-1.2X0.4-1.5X0.7

H9ML shield holes:2x 998-04440

SL0408
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0407
TH-NSP
SL-1.2X0.4-1.5X0.7

SSD shield holes:2x 998-04440

SL0410
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0409
TH-NSP
SL-1.2X0.4-1.5X0.7

HDMI shield holes:2x 998-04440

SL0420
TH-NSP
SL-1.2X0.4-1.5X0.7

SL0421
TH-NSP
SL-1.2X0.4-1.5X0.7

BOM_COST_GROUP=MECHANICALS

SYNC_MASTER=Mary
SYNC_DATE=04/26/2018

PAGE TITLE
PD Parts

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BRANCH dvt-1
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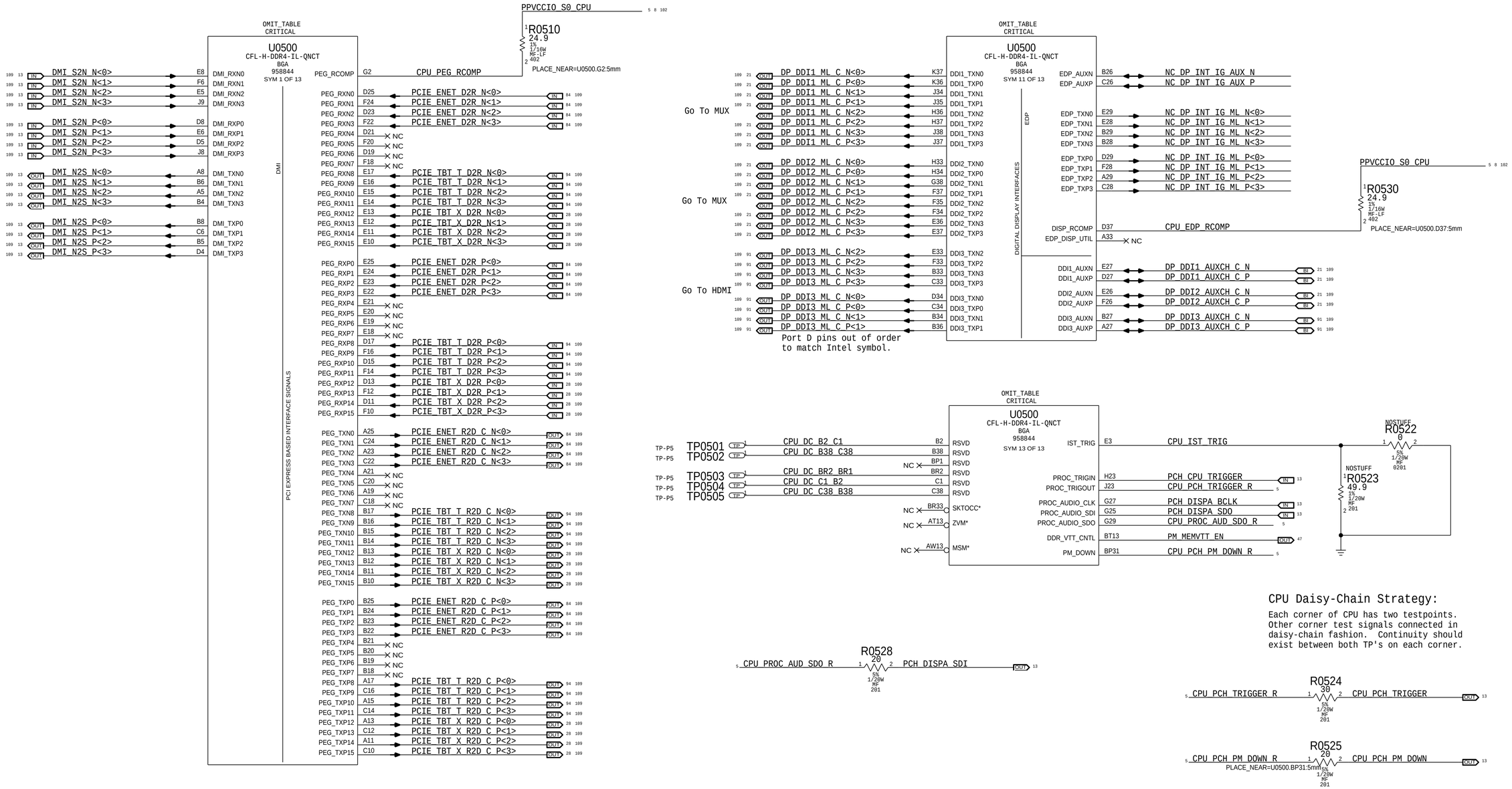

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER: 051-02424
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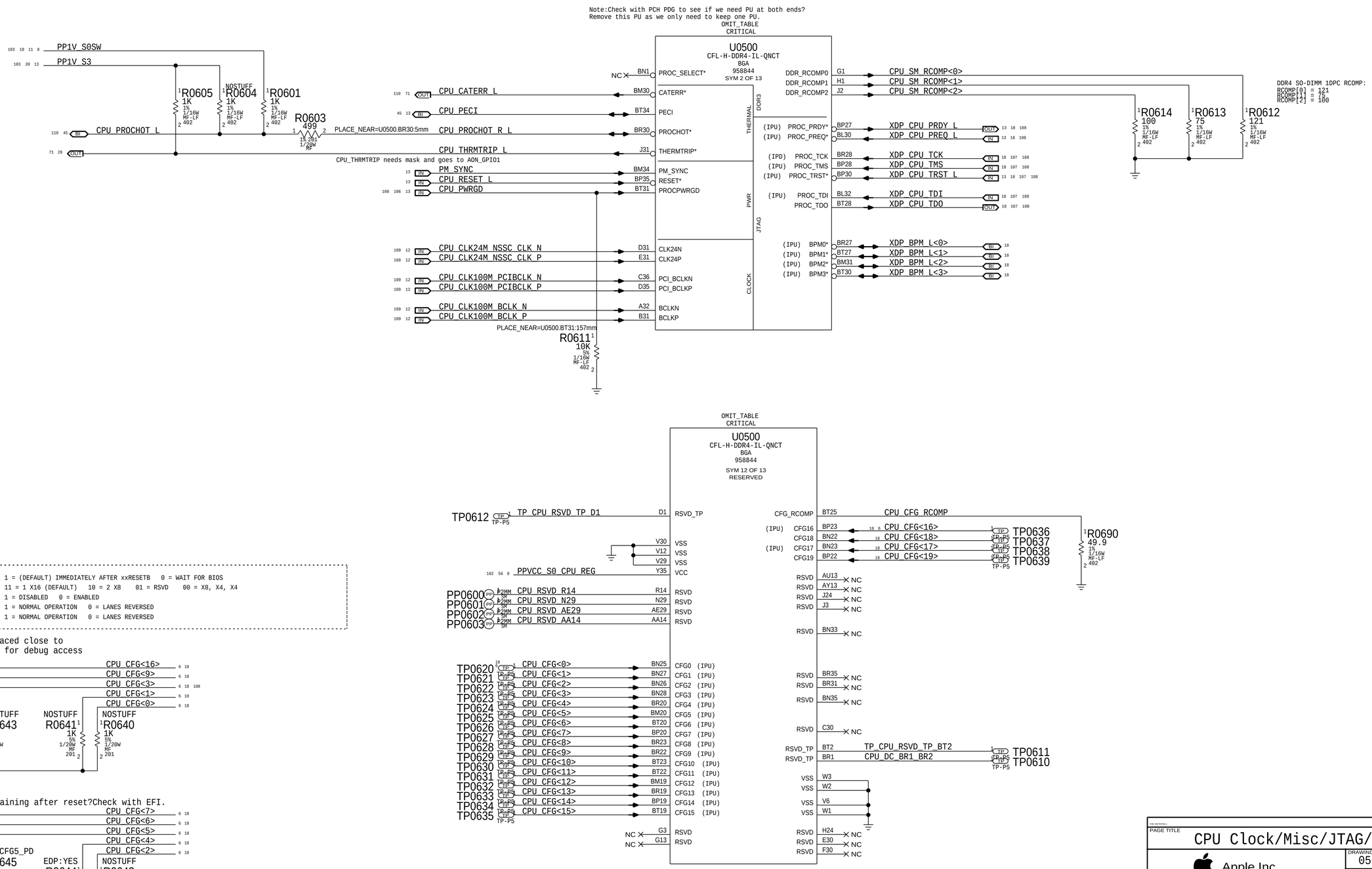

BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.

PAGE TITLE
CPU Clock/Misc/JTAG/CFG

Apple Inc.

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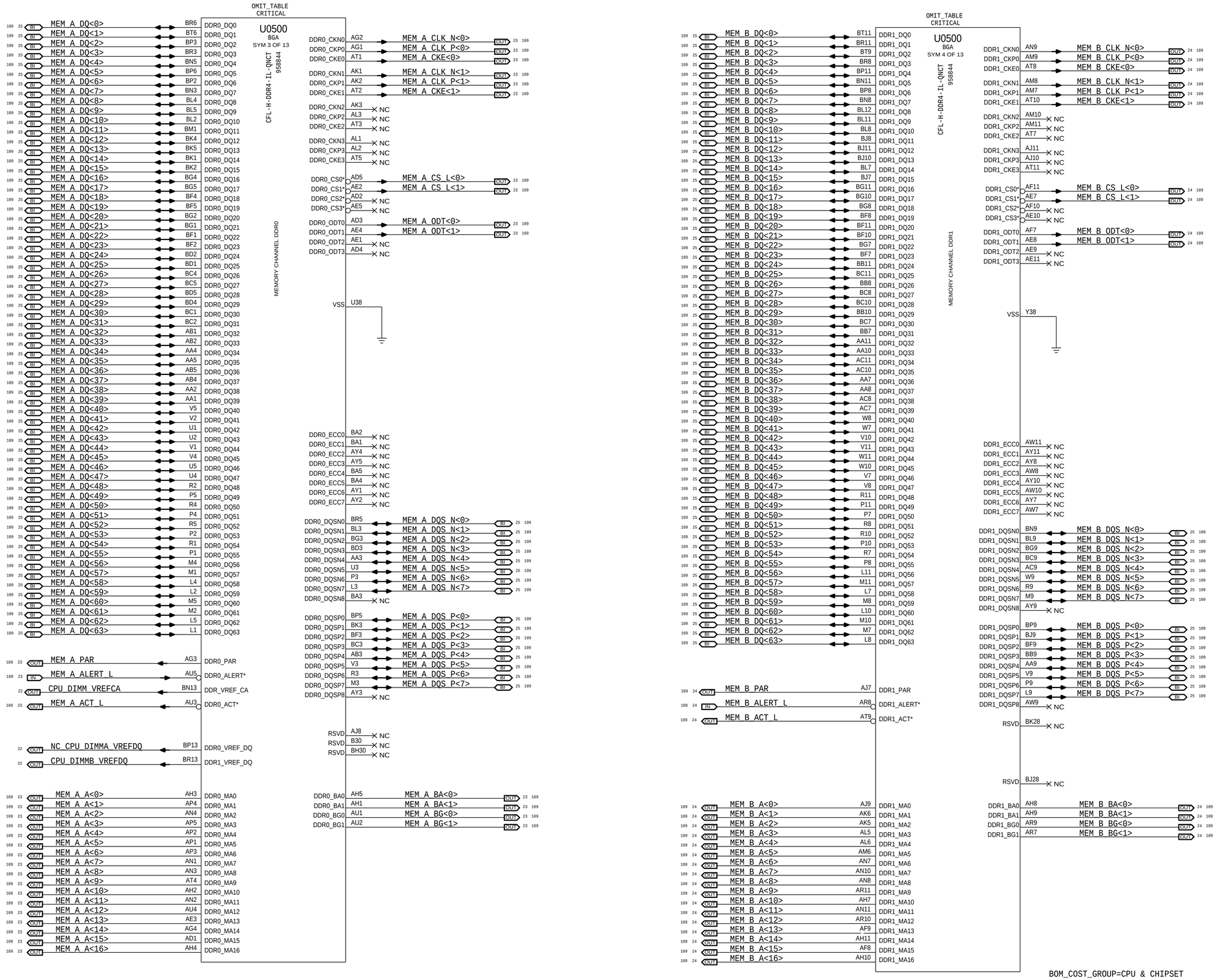

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

CPU DDR4 Interfaces

Apple Inc.

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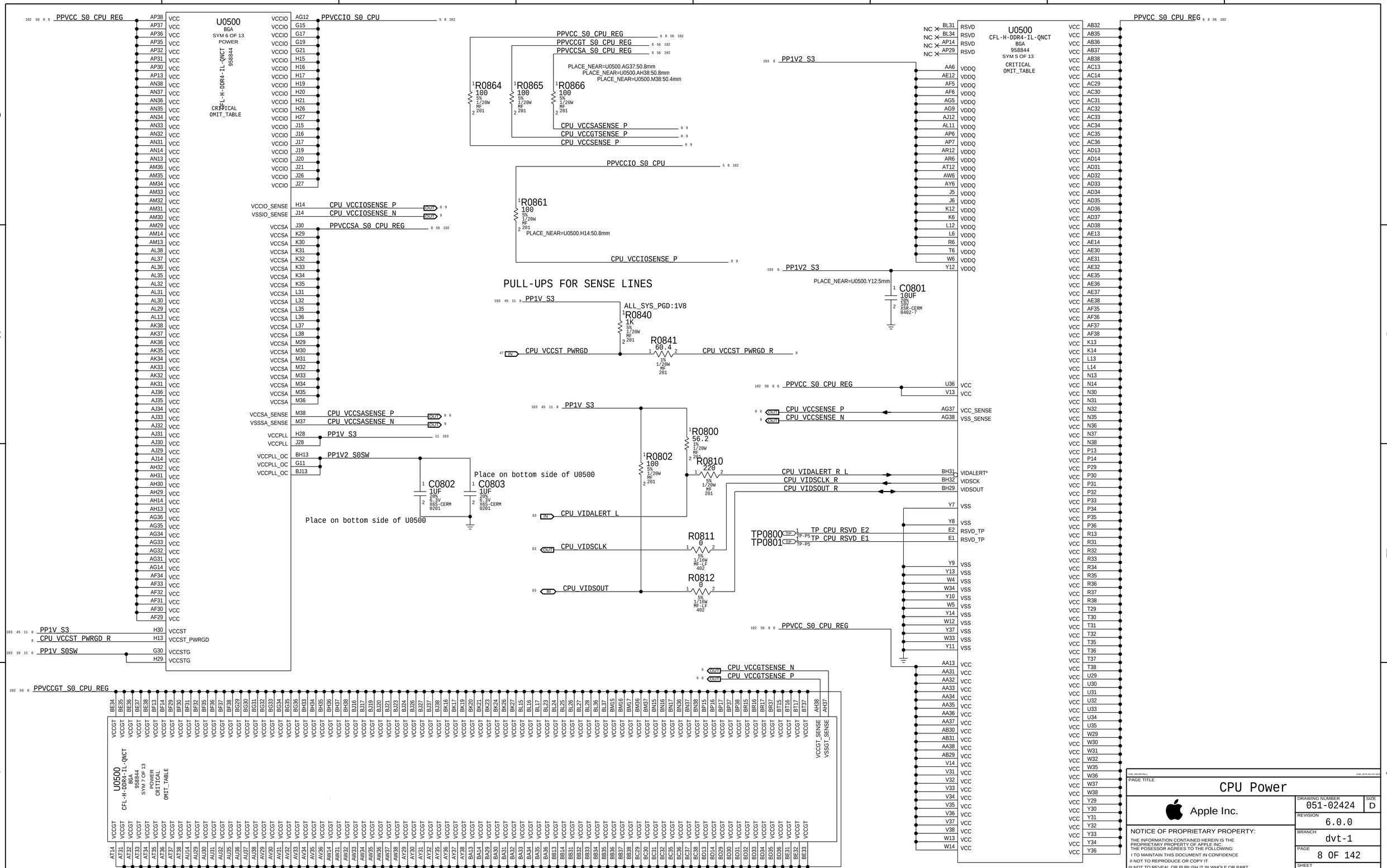

PAGE TITLE

CPU Power

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

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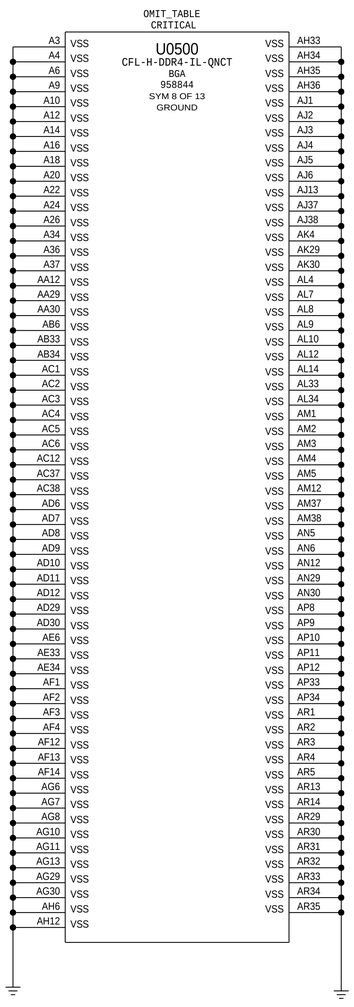

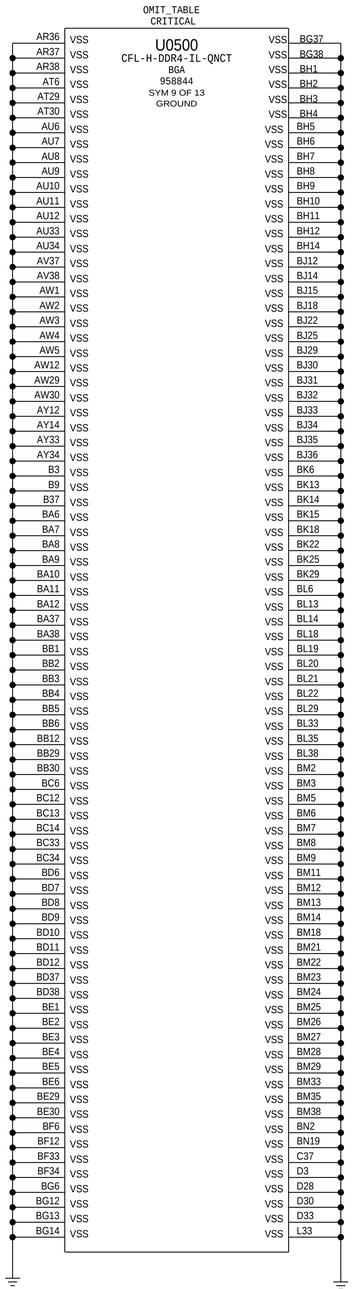

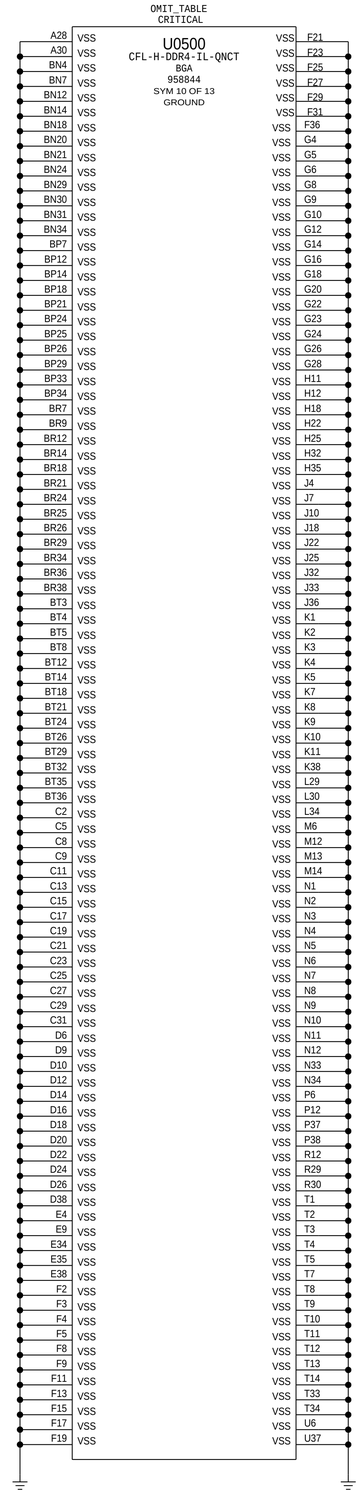

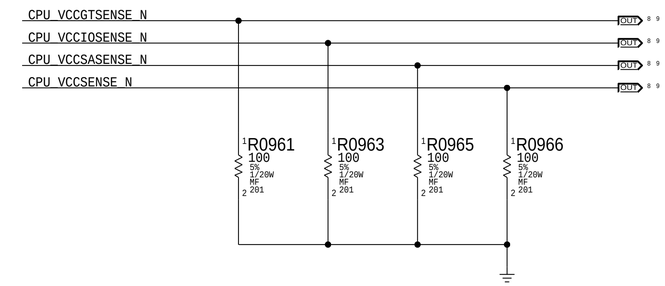

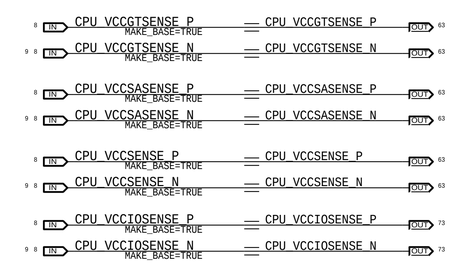

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

CPU Ground

Apple Inc.

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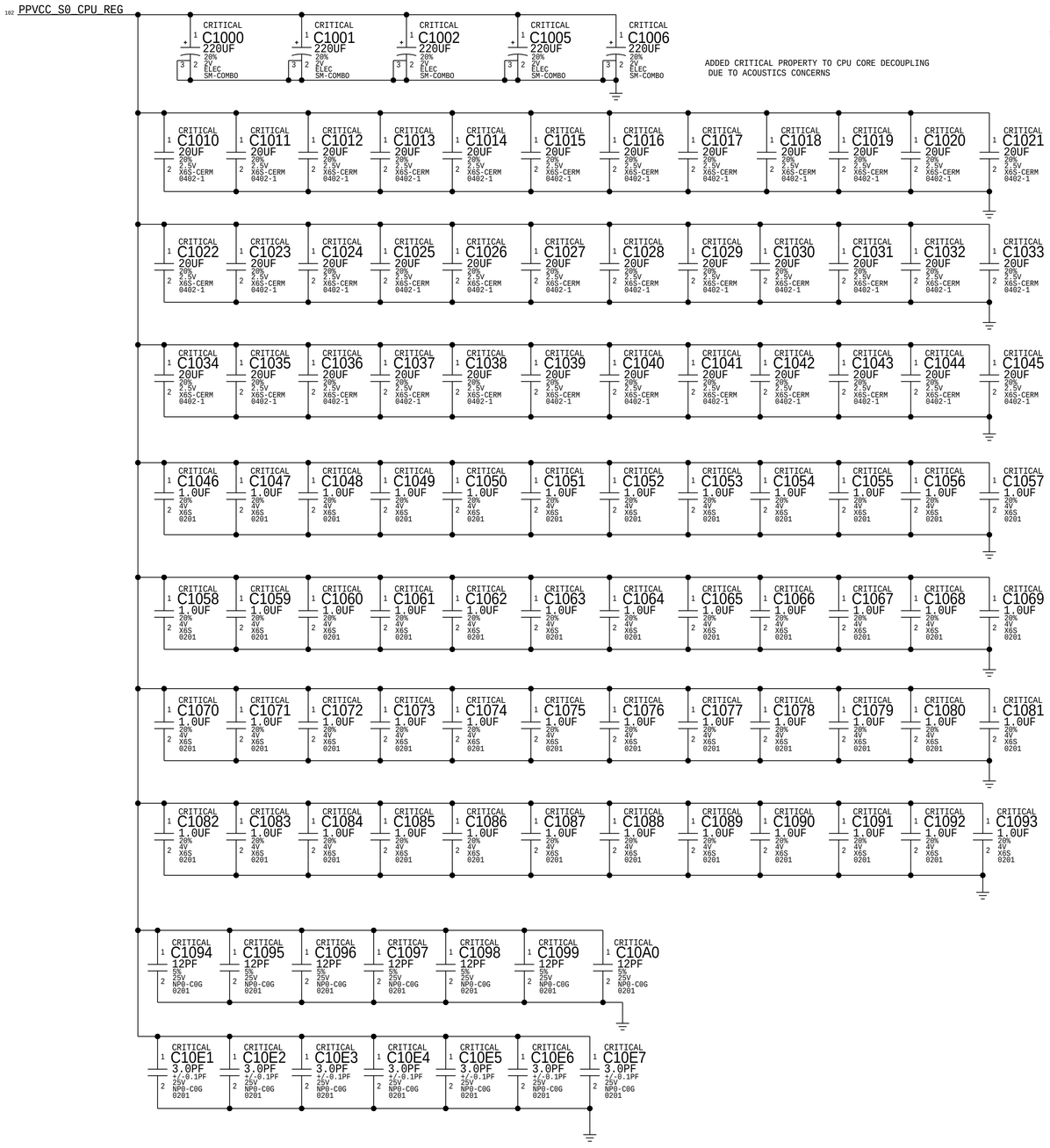
CPU VCORE DECOUPLING

Intel Recommendation:3x 330uF near CPU
5x 47uF 0805 @ board edge
12x 22UF 0603,21x 10uF 0402,24x 1uF 0201,24x 0201(placeholder) @ back side

Apple Implementation:5x 220uF
36x 20uF
48x 1uF
7x 12pF and 3pF

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.

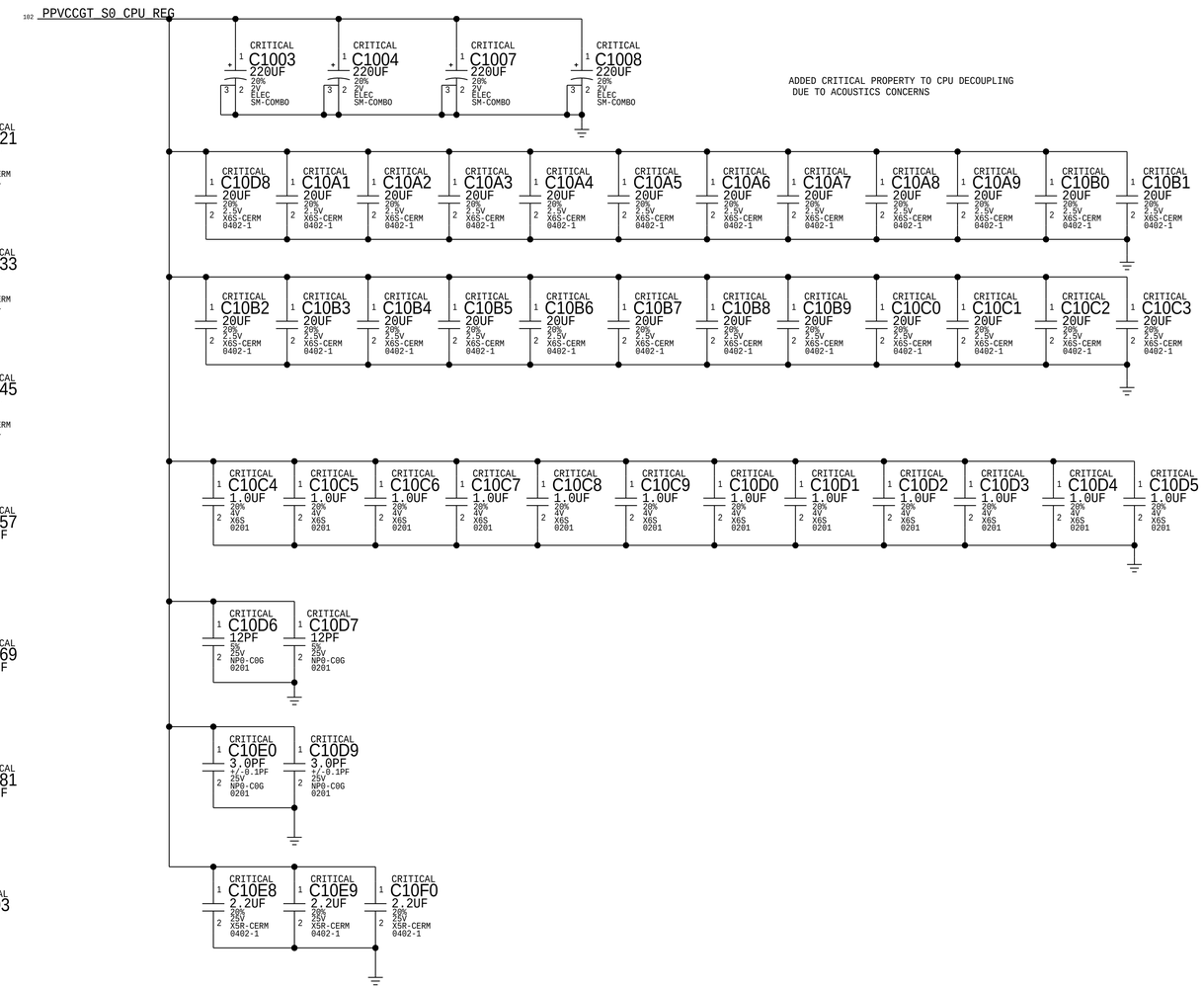


CPU GT DECOUPLING

INTEL RECOMMENDATION:2X 220uF Near CPU
3X 47uF 0805,7x 22uF 0603 @ board edge
10x 10uF 0402,12x 1uF 0201 @ back side

Apple Implementation: 4x 220uF
24x 20uF
12x 1uF
2x 12pF and 3pF

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: CPU Decoupling 1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

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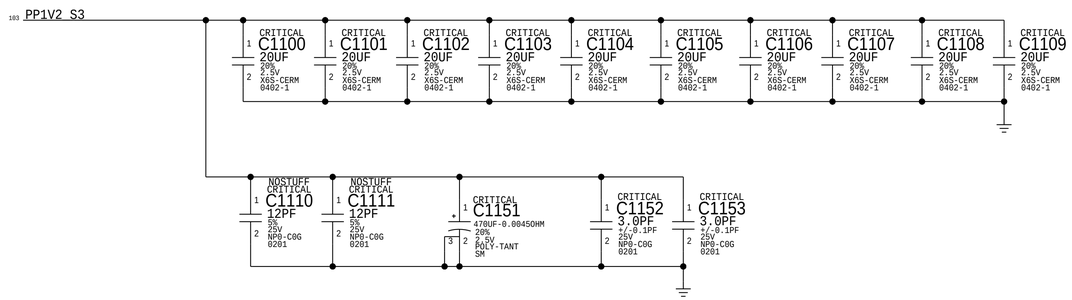
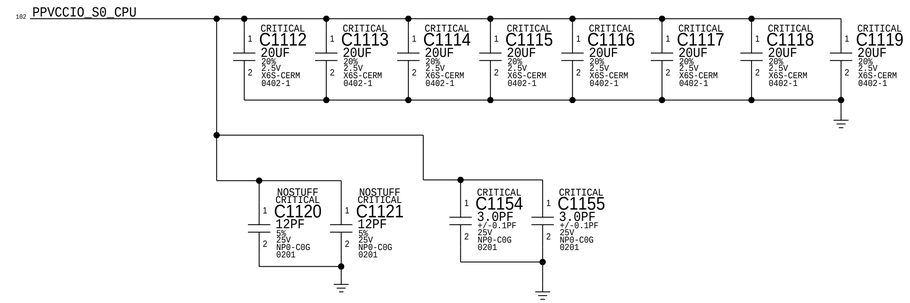
Memory (CPU VCCDDR) DECOUPLING

INTEL RECOMMENDATION:4X 22uF 0603,11x 10uF 0402 (back side)
Apple Implementation:10x 20uF
2x 12pF and 3pF (NO STUFF)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



CPU VCCIO DECOUPLING

Intel Recommendation:2x 47UF 0805 near VR ouput
3x 10uF 0402,3x 0402 placeholder @ back side
Apple Implementation:8x 20uF
2x 12pF and 3pF (NO STUFF)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.

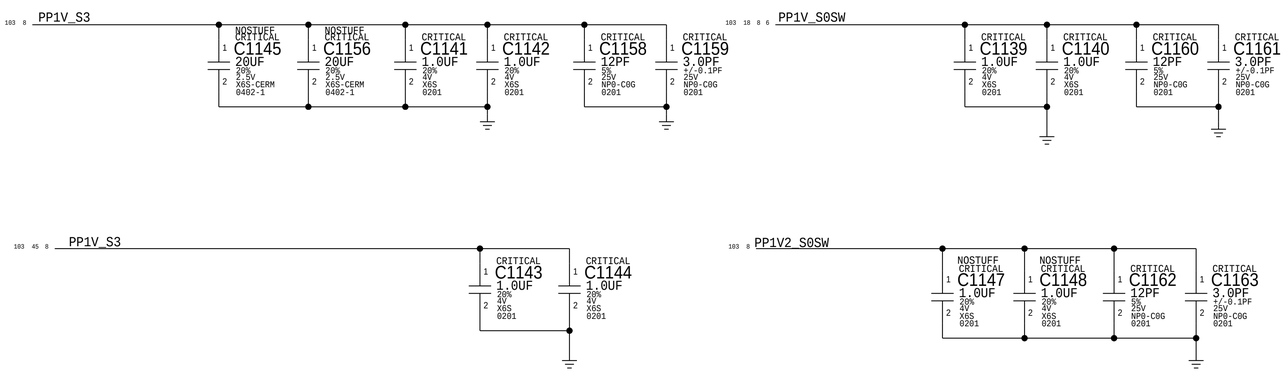


CPU VCCST / VCCSTG / VCCPLL / VCCPLL_OC DECOUPLING

Intel Recommendation: VCCST: 1x 1uF 0201
VCCSTG: 1x 1uF 0201
VCCPLL: 1x 1uF 0201,1x 22uF/47uF 0805 placeholder
VCCPLL_OC: 2x 1uF 0201

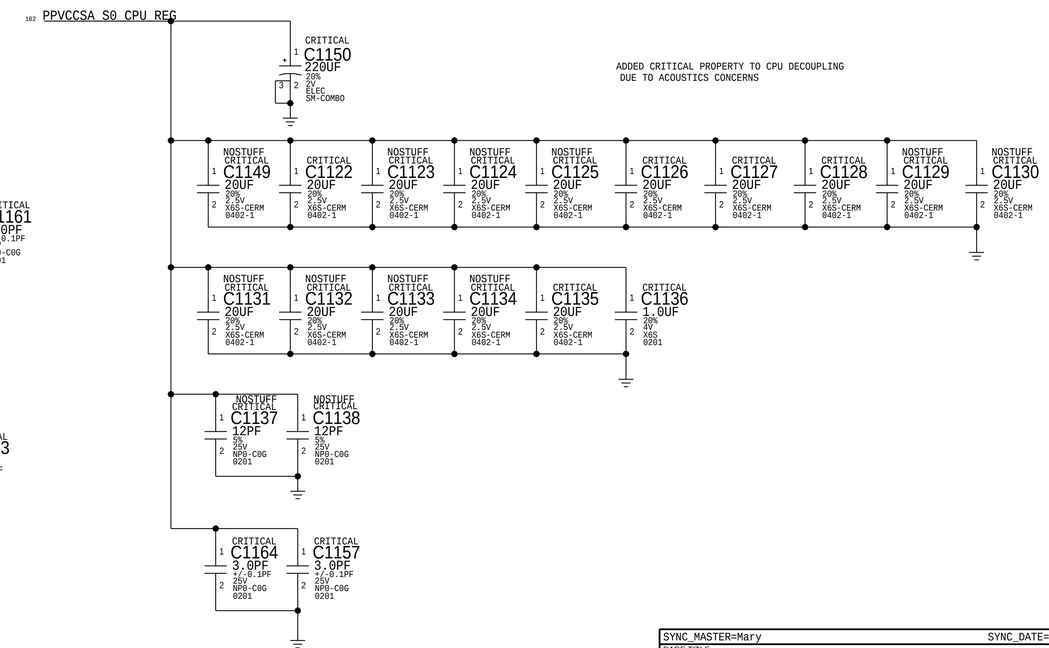
Apple Iimplementation: VCCST: 2x 1uF
VCCSTG: 2x 1uF
VCCPLL: 2x 20uF,2x 1uF
VCCPLL_OC: 2x 1uF

Layout Note: All these Must be Ground referenced.
VCCSTG board routing resistance from BGA to gate should less than 10mOhm.
Do not route VCCSTG closet adjcent layer over any power net other than GND.



CPU VCCSA DECOUPLING

Intel Recommendation:2x 47uF 0805 near CPU
2x 47uF 0805,2x 22uF 0603 @ board edge
7x 10uF 0402,1x 1uF 0201 @ backside
Apple Implementation:1x 220uF
5x 20uF
1x 1uF
2x 12pF and 3pF (NO STUFF)



ADDED CRITICAL PROPERTY TO CPU DECOUPLING
DUE TO ACOUSTICS CONCERNS

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: CPU Decoupling 2

Apple Inc.

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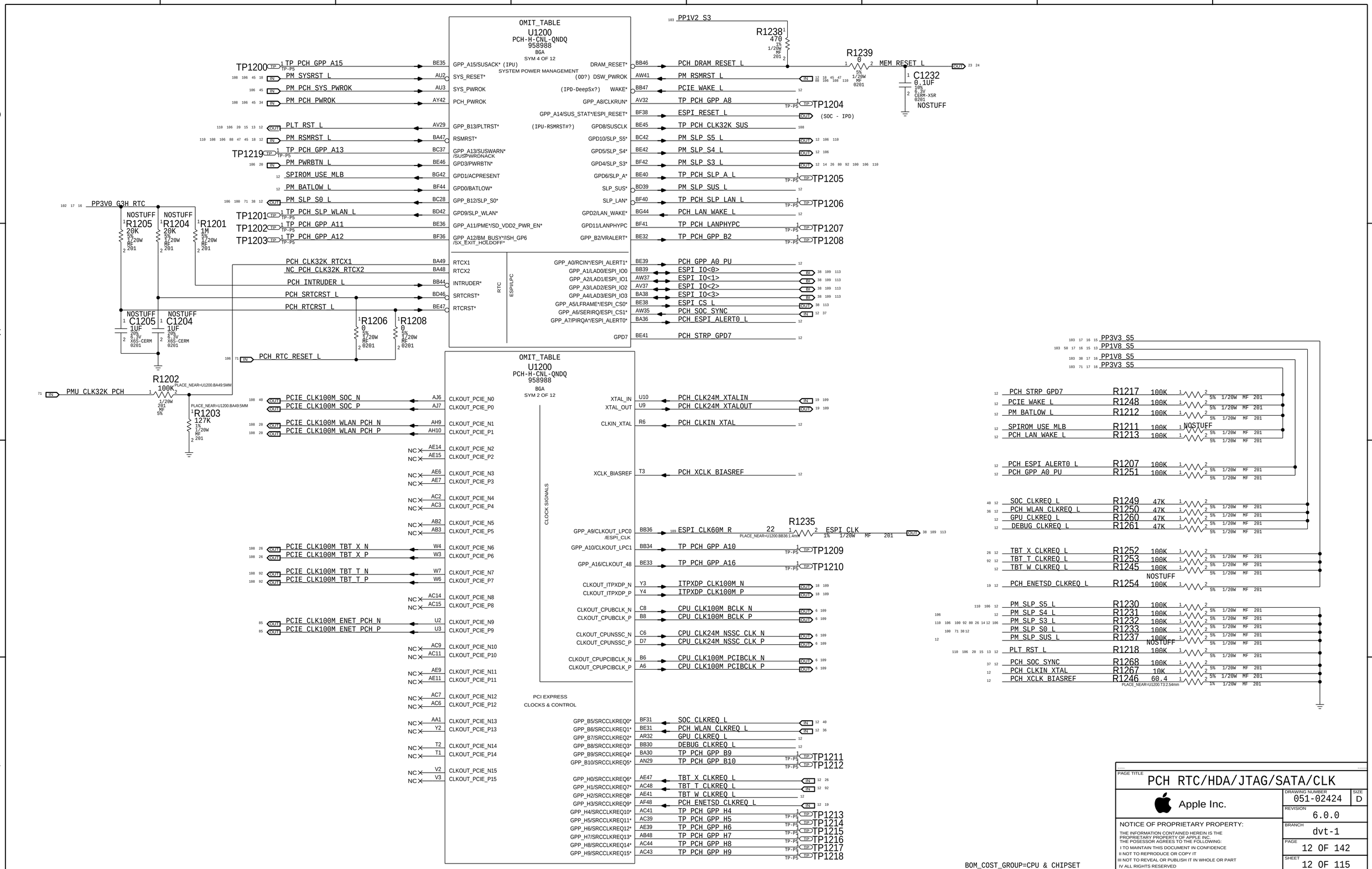
OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 4 OF 12
SYSTEM POWER MANAGEMENT
GPP_A15/SUSACK* (IPU)
SYS_RESET*
SYS_PWROK
PCH_PWROK
GPP_B13/PLTRST*
RSMRST*
GPP_A13/SUSWARN* /SUSPWRDNACK
GPD3/PWRBTN*
GPD1/ACPRESENT
GPD0/BATLOW*
GPP_B12/SLP_S0*
GPD9/SLP_WLAN*
GPP_A11/PME*/SD_VDD2_PWR_EN*
GPP_A12/BM_BUSY*/ISH_GP6 /SX_EXIT_HOLDOFF*
DRAM_RESET*
(OD?) DSW_PWROK
(IPD-DeepSx?) WAKE*
GPP_A8/CLKRUN*
GPP_A14/SUS_STAT*/ESPI_RESET*
(IPU-RSMRST#?) GPD8/SUSCLK
GPD10/SLP_S5*
GPD5/SLP_S4*
GPD4/SLP_S3*
GPD6/SLP_A*
SLP_SUS*
SLP_LAN*
GPD2/LAN_WAKE*
GPD11/LANPHYPC
GPP_B2/VRALERT*
RTCX1
RTCX2
INTRUDER*
SRTCRST*
RTCRST*
RTC
ESPI/LPC
GPP_A0/RCIN*/ESPI_ALERT1*
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME*/ESPI_CS0*
GPP_A6/SERIRQ/ESPI_CS1*
GPP_A7/PIRQA*/ESPI_ALERT0*
GPD7
PP1V2 S3
R1238 470 1% 1/20W MF 201
R1239 0 5% 1/20W MF 0201
MEM_RESET_L
C1232 0.1UF 10% 6.3V CERM-X5R 0201 NOSTUFF
TP1200 TP_PCH_GPP_A15
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PLT_RST_L
PM_RSMRST_L
TP1219 TP_PCH_GPP_A13
PM_PWRBTN_L
SPIROM_USE_MLB
PM_BATLOW_L
PM_SLP_S0_L
TP1201 TP_PCH_SLP_WLAN_L
TP1202 TP_PCH_GPP_A11
TP1203 TP_PCH_GPP_A12
PCH_DRAM_RESET_L
PM_RSMRST_L
PCIE_WAKE_L
TP_PCH_GPP_A8
TP1204
ESPI_RESET_L
(SOC - IPD)
TP_PCH_CLK32K_SUS
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PCH_SLP_A_L
TP1205
PM_SLP_SUS_L
TP_PCH_SLP_LAN_L
TP1206
PCH_LAN_WAKE_L
TP_PCH_LANPHYPC
TP1207
TP_PCH_GPP_B2
TP1208
PCH_GPP_A0_PU
ESPI_IO<0>
ESPI_IO<1>
ESPI_IO<2>
ESPI_IO<3>
ESPI_CS_L
PCH_SOC_SYNC
PCH_ESPI_ALERT0_L
PCH_STRP_GPD7
PP3V0_G3H_RTC
NOSTUFF R1205 20K 5% 1/20W MF 201
NOSTUFF R1204 20K 5% 1/20W MF 201
R1201 1M 5% 1/20W MF 201
PCH_CLK32K_RTCX1
NC_PCH_CLK32K_RTCX2
PCH_INTRUDER_L
PCH_SRTCRST_L
PCH_RTCRST_L
NOSTUFF C1205 1UF 20% 6.3V X6S-CERM 0201
NOSTUFF C1204 1UF 20% 6.3V X6S-CERM 0201
R1206 0 5% 1/20W MF 0201
R1208 0 5% 1/20W MF 0201
PCH_RTC_RESET_L
R1202 100K 1/20W MF 201 5%
PMU_CLK32K_PCH
R1203 127K 1% 1/20W MF 201
OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 2 OF 12
CLOCK SIGNALS
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
CLKOUT_PCIE_N8
CLKOUT_PCIE_P8
CLKOUT_PCIE_N9
CLKOUT_PCIE_P9
CLKOUT_PCIE_N10
CLKOUT_PCIE_P10
CLKOUT_PCIE_N11
CLKOUT_PCIE_P11
CLKOUT_PCIE_N12
CLKOUT_PCIE_P12
CLKOUT_PCIE_N13
CLKOUT_PCIE_P13
CLKOUT_PCIE_N14
CLKOUT_PCIE_P14
CLKOUT_PCIE_N15
CLKOUT_PCIE_P15
PCIE_CLK100M_SOC_N
PCIE_CLK100M_SOC_P
PCIE_CLK100M_WLAN_PCH_N
PCIE_CLK100M_WLAN_PCH_P
PCIE_CLK100M_TBT_X_N
PCIE_CLK100M_TBT_X_P
PCIE_CLK100M_TBT_T_N
PCIE_CLK100M_TBT_T_P
PCIE_CLK100M_ENET_PCH_N
PCIE_CLK100M_ENET_PCH_P
PCI EXPRESS
CLOCKS & CONTROL
XTAL_IN
XTAL_OUT
CLKIN_XTAL
XCLK_BIASREF
PCH_CLK24M_XTALIN
PCH_CLK24M_XTALOUT
PCH_CLKIN_XTAL
PCH_XCLK_BIASREF
GPP_A9/CLKOUT_LPC0 /ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A16/CLKOUT_48
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_CPUBCLK_N
CLKOUT_CPUBCLK_P
CLKOUT_CPUNSSC_N
CLKOUT_CPUNSSC_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_CPUPCIBCLK_P
R1235 22 1% 1/20W MF 201
ESPI_CLK60M_R
ESPI_CLK
TP_PCH_GPP_A10
TP1209
TP_PCH_GPP_A16
TP1210
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
CPU_CLK100M_BCLK_N
CPU_CLK100M_BCLK_P
CPU_CLK24M_NSSC_CLK_N
CPU_CLK24M_NSSC_CLK_P
CPU_CLK100M_PCIBCLK_N
CPU_CLK100M_PCIBCLK_P
SOC_CLKREQ_L
PCH_WLAN_CLKREQ_L
GPU_CLKREQ_L
DEBUG_CLKREQ_L
TP_PCH_GPP_B9
TP_PCH_GPP_B10
TP1211
TP1212
TBT_X_CLKREQ_L
TBT_T_CLKREQ_L
TBT_W_CLKREQ_L
PCH_ENETSD_CLKREQ_L
TP_PCH_GPP_H4
TP_PCH_GPP_H5
TP_PCH_GPP_H6
TP_PCH_GPP_H7
TP_PCH_GPP_H8
TP_PCH_GPP_H9
TP1213
TP1214
TP1215
TP1216
TP1217
TP1218
PP3V3_S5
PP1V8_S5
R1217 100K
R1248 100K
R1212 100K
R1211 100K
R1213 100K
R1207 100K
R1251 100K
R1249 47K
R1250 47K
R1260 47K
R1261 47K
R1252 100K
R1253 100K
R1245 100K
R1254 100K
R1230 100K
R1231 100K
R1232 100K
R1233 100K
R1237 100K
R1218 100K
R1268 100K
R1267 10K
R1246 60.4 1%
PCH_CLKIN_XTAL
PCH_XCLK_BIASREF
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK
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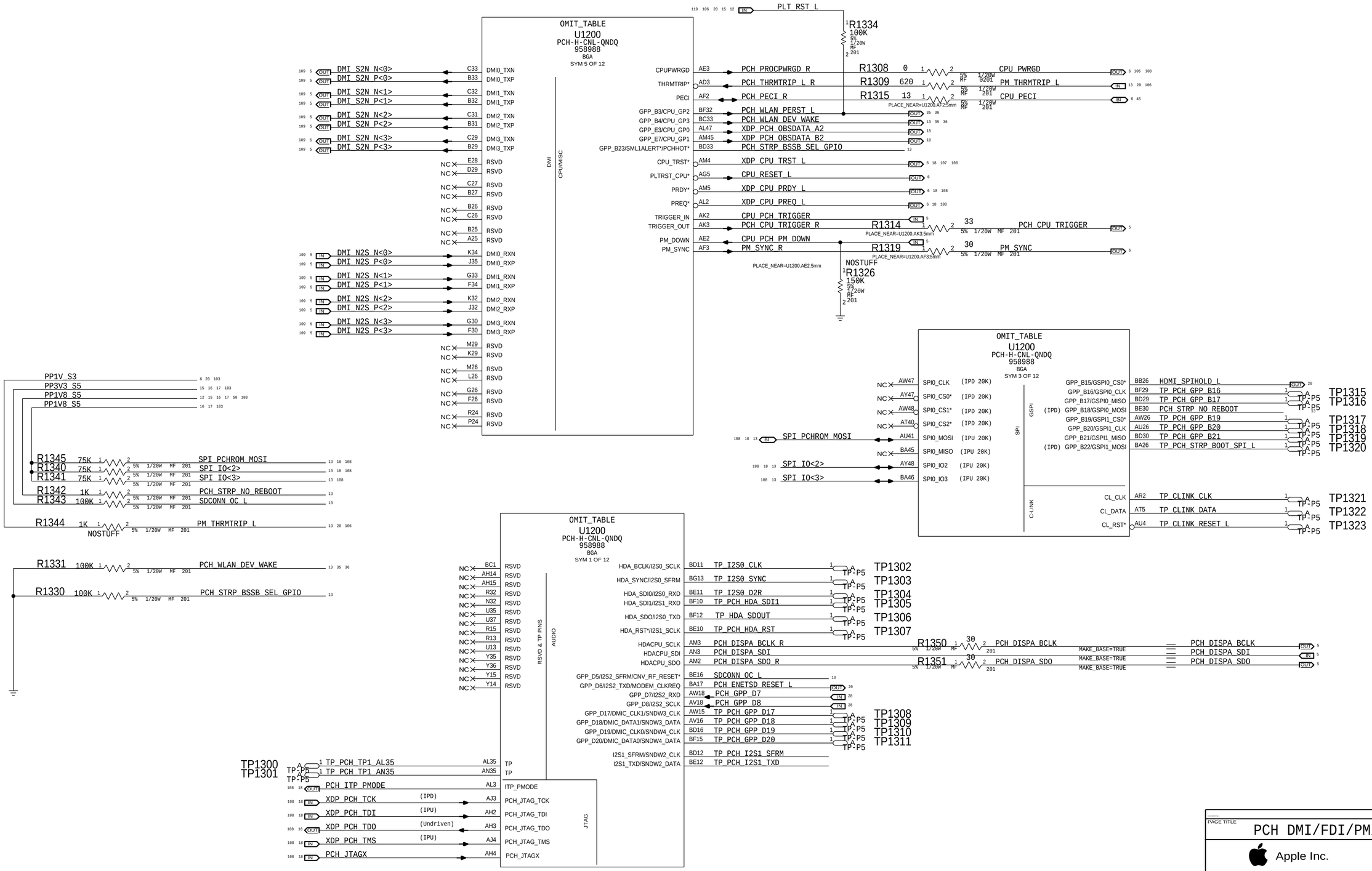

PAGE TITLE
PCH DMI/FDI/PM/GFX/PCI

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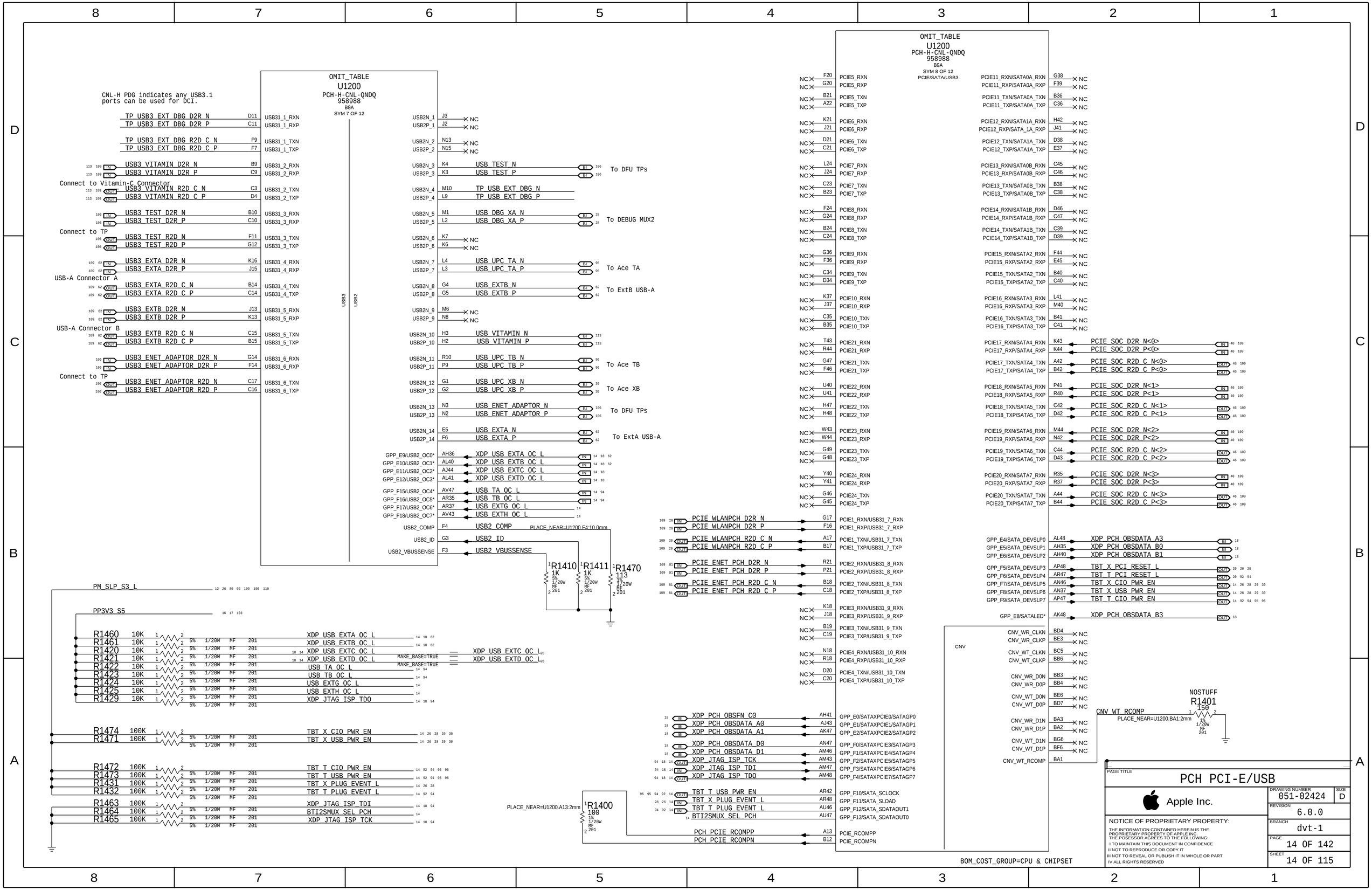
OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 7 OF 12
CNL-H PDG indicates any USB3.1 ports can be used for DCI.
TP_USB3_EXT_DBG_D2R_N D11 USB31_1_RXN
TP_USB3_EXT_DBG_D2R_P C11 USB31_1_RXP
TP_USB3_EXT_DBG_R2D_C_N F9 USB31_1_TXN
TP_USB3_EXT_DBG_R2D_C_P F7 USB31_1_TXP
USB3_VITAMIN_D2R_N B9 USB31_2_RXN
USB3_VITAMIN_D2R_P C9 USB31_2_RXP
Connect to Vitamin-C Connector
USB3_VITAMIN_R2D_C_N C3 USB31_2_TXN
USB3_VITAMIN_R2D_C_P D4 USB31_2_TXP
USB3_TEST_D2R_N B10 USB31_3_RXN
USB3_TEST_D2R_P C10 USB31_3_RXP
Connect to TP
USB3_TEST_R2D_N F11 USB31_3_TXN
USB3_TEST_R2D_P G12 USB31_3_TXP
USB3_EXTA_D2R_N K16 USB31_4_RXN
USB3_EXTA_D2R_P J15 USB31_4_RXP
USB-A Connector A
USB3_EXTA_R2D_C_N B14 USB31_4_TXN
USB3_EXTA_R2D_C_P C14 USB31_4_TXP
USB3_EXTB_D2R_N J13 USB31_5_RXN
USB3_EXTB_D2R_P K13 USB31_5_RXP
USB-A Connector B
USB3_EXTB_R2D_C_N C15 USB31_5_TXN
USB3_EXTB_R2D_C_P B15 USB31_5_TXP
USB3_ENET_ADAPTOR_D2R_N G14 USB31_6_RXN
USB3_ENET_ADAPTOR_D2R_P F14 USB31_6_RXP
Connect to TP
USB3_ENET_ADAPTOR_R2D_N C17 USB31_6_TXN
USB3_ENET_ADAPTOR_R2D_P C16 USB31_6_TXP
USB3
USB2
USB2N_1 J3 NC
USB2P_1 J2 NC
USB2N_2 N13 NC
USB2P_2 N15 NC
USB2N_3 K4 USB_TEST_N To DFU TPs
USB2P_3 K3 USB_TEST_P
USB2N_4 M10 TP_USB_EXT_DBG_N
USB2P_4 L9 TP_USB_EXT_DBG_P
USB2N_5 M1 USB_DBG_XA_N To DEBUG MUX2
USB2P_5 L2 USB_DBG_XA_P
USB2N_6 K7 NC
USB2P_6 K6 NC
USB2N_7 L4 USB_UPC_TA_N To Ace TA
USB2P_7 L3 USB_UPC_TA_P
USB2N_8 G4 USB_EXTB_N To ExtB USB-A
USB2P_8 G5 USB_EXTB_P
USB2N_9 M6 NC
USB2P_9 N8 NC
USB2N_10 H3 USB_VITAMIN_N
USB2P_10 H2 USB_VITAMIN_P
USB2N_11 R10 USB_UPC_TB_N To Ace TB
USB2P_11 P9 USB_UPC_TB_P
USB2N_12 G1 USB_UPC_XB_N To Ace XB
USB2P_12 G2 USB_UPC_XB_P
USB2N_13 N3 USB_ENET_ADAPTOR_N To DFU TPs
USB2P_13 N2 USB_ENET_ADAPTOR_P
USB2N_14 E5 USB_EXTA_N To ExtA USB-A
USB2P_14 F6 USB_EXTA_P
GPP_E9/USB2_OC0* AH36 XDP_USB_EXTA_OC_L
GPP_E10/USB2_OC1* AL40 XDP_USB_EXTB_OC_L
GPP_E11/USB2_OC2* AJ44 XDP_USB_EXTC_OC_L
GPP_E12/USB2_OC3* AL41 XDP_USB_EXTD_OC_L
GPP_F15/USB2_OC4* AV47 USB_TA_OC_L
GPP_F16/USB2_OC5* AR35 USB_TB_OC_L
GPP_F17/USB2_OC6* AR37 USB_EXTG_OC_L
GPP_F18/USB2_OC7* AV43 USB_EXTH_OC_L
USB2_COMP F4 USB2_COMP PLACE_NEAR=U1200.F4:10.0mm
USB2_ID G3 USB2_ID
USB2_VBUSSENSE F3 USB2_VBUSSENSE
R1410 1K 5% 1/20W MF 201
R1411 1K 5% 1/20W MF 201
R1470 113 1% 1/20W MF 201
PM_SLP_S3_L
PP3V3_S5
R1460 10K 5% 1/20W MF 201 XDP_USB_EXTA_OC_L
R1461 10K 5% 1/20W MF 201 XDP_USB_EXTB_OC_L
R1420 10K 5% 1/20W MF 201 XDP_USB_EXTC_OC_L
R1421 10K 5% 1/20W MF 201 XDP_USB_EXTD_OC_L
R1422 10K 5% 1/20W MF 201 USB_TA_OC_L
R1423 10K 5% 1/20W MF 201 USB_TB_OC_L
R1424 10K 5% 1/20W MF 201 USB_EXTG_OC_L
R1425 10K 5% 1/20W MF 201 USB_EXTH_OC_L
R1429 10K 5% 1/20W MF 201 XDP_JTAG_ISP_TDO
MAKE_BASE=TRUE
XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L
R1474 100K 5% 1/20W MF 201 TBT_X_CIO_PWR_EN
R1471 100K 5% 1/20W MF 201 TBT_X_USB_PWR_EN
R1472 100K 5% 1/20W MF 201 TBT_T_CIO_PWR_EN
R1473 100K 5% 1/20W MF 201 TBT_T_USB_PWR_EN
R1431 100K 5% 1/20W MF 201 TBT_X_PLUG_EVENT_L
R1432 100K 5% 1/20W MF 201 TBT_T_PLUG_EVENT_L
R1463 100K 5% 1/20W MF 201 XDP_JTAG_ISP_TDI
R1464 100K 5% 1/20W MF 201 BTI2SMUX_SEL_PCH
R1465 100K 5% 1/20W MF 201 XDP_JTAG_ISP_TCK
PLACE_NEAR=U1200.A13:2mm
R1400 100 1% 1/20W MF 201
OMIT_TABLE
U1200
PCH-H-CNL-QNDQ
958988
BGA
SYM 8 OF 12
PCIE/SATA/USB3
PCIE5_RXN F20 NC
PCIE5_RXP G20 NC
PCIE5_TXN B21 NC
PCIE5_TXP A22 NC
PCIE6_RXN K21 NC
PCIE6_RXP J21 NC
PCIE6_TXN D21 NC
PCIE6_TXP C21 NC
PCIE7_RXN L24 NC
PCIE7_RXP J24 NC
PCIE7_TXN C23 NC
PCIE7_TXP B23 NC
PCIE8_RXN F24 NC
PCIE8_RXP G24 NC
PCIE8_TXN B24 NC
PCIE8_TXP C24 NC
PCIE9_RXN G36 NC
PCIE9_RXP F36 NC
PCIE9_TXN C34 NC
PCIE9_TXP D34 NC
PCIE10_RXN K37 NC
PCIE10_RXP J37 NC
PCIE10_TXN C35 NC
PCIE10_TXP B35 NC
PCIE21_RXN T43 NC
PCIE21_RXP R44 NC
PCIE21_TXN G47 NC
PCIE21_TXP F46 NC
PCIE22_RXN U40 NC
PCIE22_RXP U41 NC
PCIE22_TXN H47 NC
PCIE22_TXP H48 NC
PCIE23_RXN W43 NC
PCIE23_RXP W44 NC
PCIE23_TXN G49 NC
PCIE23_TXP G48 NC
PCIE24_RXN Y40 NC
PCIE24_RXP Y41 NC
PCIE24_TXN G46 NC
PCIE24_TXP G45 NC
PCIE_WLANPCH_D2R_N G17 PCIE1_RXN/USB31_7_RXN
PCIE_WLANPCH_D2R_P F16 PCIE1_RXP/USB31_7_RXP
PCIE_WLANPCH_R2D_C_N A17 PCIE1_TXN/USB31_7_TXN
PCIE_WLANPCH_R2D_C_P B17 PCIE1_TXP/USB31_7_TXP
PCIE_ENET_PCH_D2R_N R21 PCIE2_RXN/USB31_8_RXN
PCIE_ENET_PCH_D2R_P P21 PCIE2_RXP/USB31_8_RXP
PCIE_ENET_PCH_R2D_C_N B18 PCIE2_TXN/USB31_8_TXN
PCIE_ENET_PCH_R2D_C_P C18 PCIE2_TXP/USB31_8_TXP
PCIE3_RXN/USB31_9_RXN K18 NC
PCIE3_RXP/USB31_9_RXP J18 NC
PCIE3_TXN/USB31_9_TXN B19 NC
PCIE3_TXP/USB31_9_TXP C19 NC
PCIE4_RXN/USB31_10_RXN N18 NC
PCIE4_RXP/USB31_10_RXP R18 NC
PCIE4_TXN/USB31_10_TXN D20 NC
PCIE4_TXP/USB31_10_TXP C20 NC
XDP_PCH_OBSFN_C0 AH41 GPP_E0/SATAXPCIE0/SATAGP0
XDP_PCH_OBSDATA_A0 AJ43 GPP_E1/SATAXPCIE1/SATAGP1
XDP_PCH_OBSDATA_A1 AK47 GPP_E2/SATAXPCIE2/SATAGP2
XDP_PCH_OBSDATA_D0 AN47 GPP_F0/SATAXPCIE3/SATAGP3
XDP_PCH_OBSDATA_D1 AM46 GPP_F1/SATAXPCIE4/SATAGP4
XDP_JTAG_ISP_TCK AM43 GPP_F2/SATAXPCIE5/SATAGP5
XDP_JTAG_ISP_TDI AM47 GPP_F3/SATAXPCIE6/SATAGP6
XDP_JTAG_ISP_TDO AM48 GPP_F4/SATAXPCIE7/SATAGP7
TBT_T_USB_PWR_EN AR42 GPP_F10/SATA_SCLOCK
TBT_X_PLUG_EVENT_L AR48 GPP_F11/SATA_SLOAD
TBT_T_PLUG_EVENT_L AU46 GPP_F12/SATA_SDATAOUT1
BTI2SMUX_SEL_PCH AU47 GPP_F13/SATA_SDATAOUT0
PCH_PCIE_RCOMPP A13 PCIE_RCOMPP
PCH_PCIE_RCOMPN B12 PCIE_RCOMPN
PCIE11_RXN/SATA0A_RXN G38 NC
PCIE11_RXP/SATA0A_RXP F39 NC
PCIE11_TXN/SATA0A_TXN B36 NC
PCIE11_TXP/SATA0A_TXP C36 NC
PCIE12_RXN/SATA1A_RXN H42 NC
PCIE12_RXP/SATA_1A_RXP J41 NC
PCIE12_TXN/SATA1A_TXN D38 NC
PCIE12_TXP/SATA1A_TXP E37 NC
PCIE13_RXN/SATA0B_RXN C45 NC
PCIE13_RXP/SATA0B_RXP C46 NC
PCIE13_TXN/SATA0B_TXN B38 NC
PCIE13_TXP/SATA0B_TXP C38 NC
PCIE14_RXN/SATA1B_RXN D46 NC
PCIE14_RXP/SATA1B_RXP C47 NC
PCIE14_TXN/SATA1B_TXN C39 NC
PCIE14_TXP/SATA1B_TXP D39 NC
PCIE15_RXN/SATA2_RXN F44 NC
PCIE15_RXP/SATA2_RXP E45 NC
PCIE15_TXN/SATA2_TXN B40 NC
PCIE15_TXP/SATA2_TXP C40 NC
PCIE16_RXN/SATA3_RXN L41 NC
PCIE16_RXP/SATA3_RXP M40 NC
PCIE16_TXN/SATA3_TXN B41 NC
PCIE16_TXP/SATA3_TXP C41 NC
PCIE17_RXN/SATA4_RXN K43 PCIE_SOC_D2R_N<0>
PCIE17_RXP/SATA4_RXP K44 PCIE_SOC_D2R_P<0>
PCIE17_TXN/SATA4_TXN A42 PCIE_SOC_R2D_C_N<0>
PCIE17_TXP/SATA4_TXP B42 PCIE_SOC_R2D_C_P<0>
PCIE18_RXN/SATA5_RXN P41 PCIE_SOC_D2R_N<1>
PCIE18_RXP/SATA5_RXP R40 PCIE_SOC_D2R_P<1>
PCIE18_TXN/SATA5_TXN C42 PCIE_SOC_R2D_C_N<1>
PCIE18_TXP/SATA5_TXP D42 PCIE_SOC_R2D_C_P<1>
PCIE19_RXN/SATA6_RXN M44 PCIE_SOC_D2R_N<2>
PCIE19_RXP/SATA6_RXP N42 PCIE_SOC_D2R_P<2>
PCIE19_TXN/SATA6_TXN C44 PCIE_SOC_R2D_C_N<2>
PCIE19_TXP/SATA6_TXP D43 PCIE_SOC_R2D_C_P<2>
PCIE20_RXN/SATA7_RXN R35 PCIE_SOC_D2R_N<3>
PCIE20_RXP/SATA7_RXP R37 PCIE_SOC_D2R_P<3>
PCIE20_TXN/SATA7_TXN A44 PCIE_SOC_R2D_C_N<3>
PCIE20_TXP/SATA7_TXP B44 PCIE_SOC_R2D_C_P<3>
GPP_E4/SATA_DEVSLP0 AL48 XDP_PCH_OBSDATA_A3
GPP_E5/SATA_DEVSLP1 AH35 XDP_PCH_OBSDATA_B0
GPP_E6/SATA_DEVSLP2 AH40 XDP_PCH_OBSDATA_B1
GPP_F5/SATA_DEVSLP3 AP48 TBT_X_PCI_RESET_L
GPP_F6/SATA_DEVSLP4 AR47 TBT_T_PCI_RESET_L
GPP_F7/SATA_DEVSLP5 AN46 TBT_X_CIO_PWR_EN
GPP_F8/SATA_DEVSLP6 AN37 TBT_X_USB_PWR_EN
GPP_F9/SATA_DEVSLP7 AP47 TBT_T_CIO_PWR_EN
GPP_E8/SATALED* AK48 XDP_PCH_OBSDATA_B3
CNV
CNV_WR_CLKN BD4 NC
CNV_WR_CLKP BE3 NC
CNV_WT_CLKN BC5 NC
CNV_WT_CLKP BB6 NC
CNV_WR_D0N BB3 NC
CNV_WR_D0P BB4 NC
CNV_WT_D0N BE6 NC
CNV_WT_D0P BD7 NC
CNV_WR_D1N BA3 NC
CNV_WR_D1P BA2 NC
CNV_WT_D1N BG6 NC
CNV_WT_D1P BF6 NC
CNV_WT_RCOMP BA1
CNV_WT_RCOMP
PLACE_NEAR=U1200.BA1:2mm
NOSTUFF
R1401 150 1% 1/20W MF 201
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
PCH PCI-E/USB
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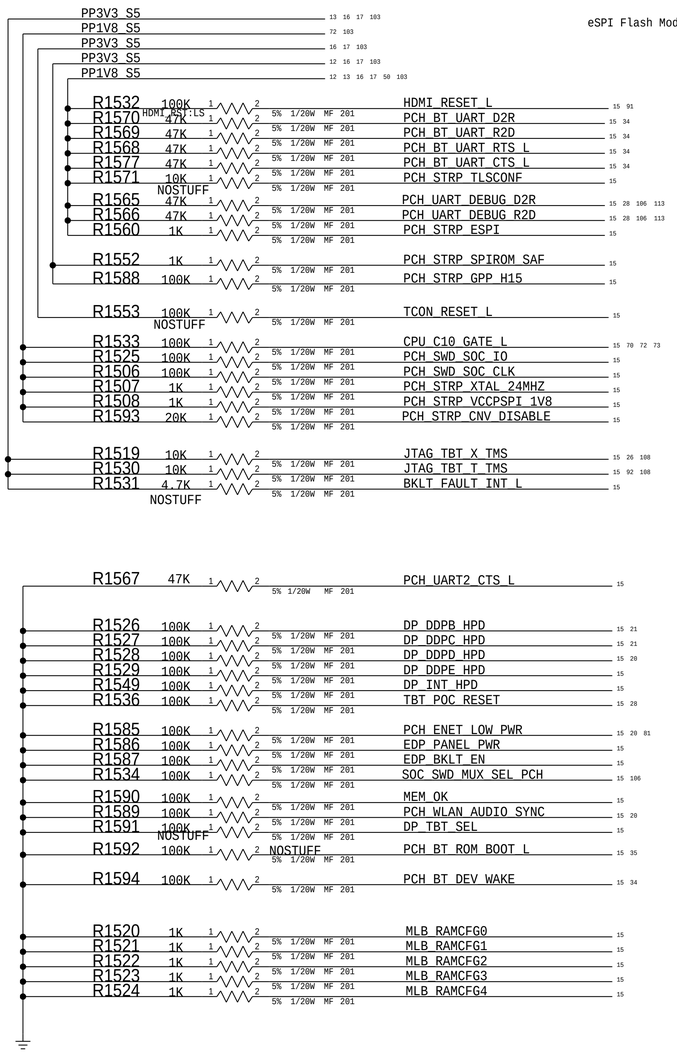
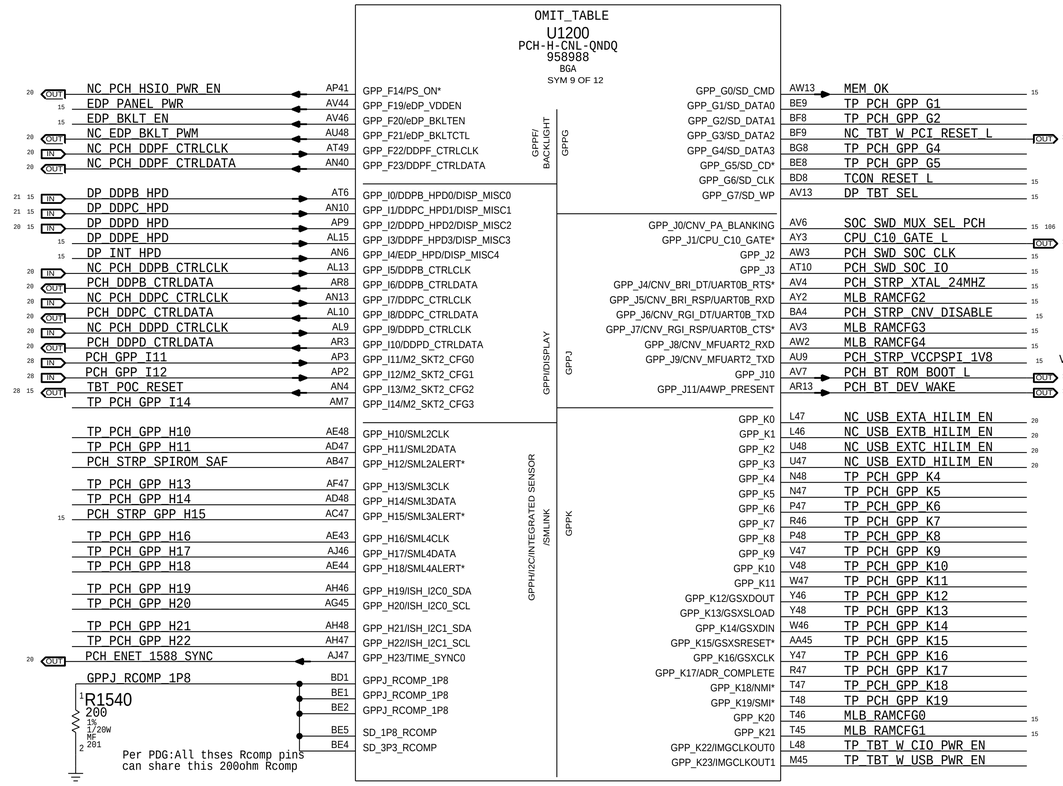
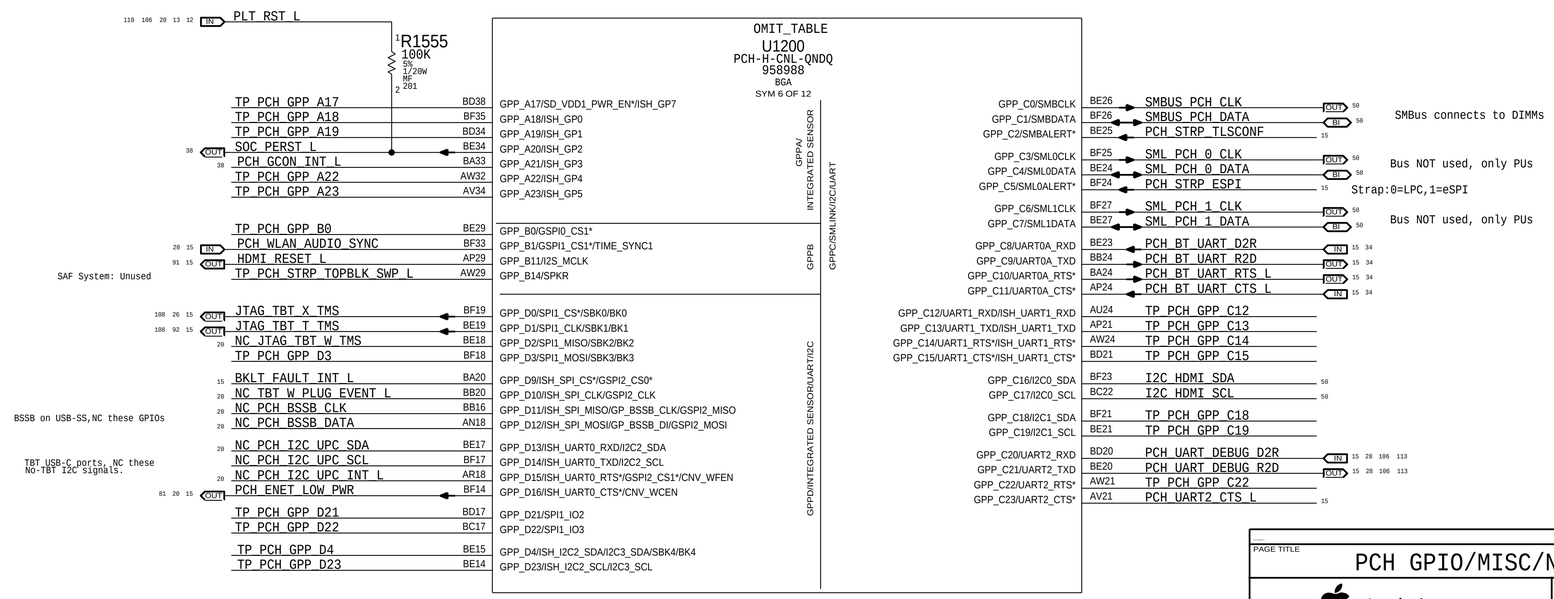


eSPI Flash Mode:0=MAF(not supported),1=SAF



If useing 38.4Mhz->PCH_STRP_XTAL38P4MHZ_L
DIMM config, no need to check RAMCFG

VCCSPI: 0=3.3V,1=1.8V



SAF System: Unused

BSSB on USB-SS,NC these GPIOs

TBT_USB-C ports, NC these NO-TBT I2C signals.

SMBus connects to DIMMs

Bus NOT used, only PUs

Strap:0=LPC,1=eSPI

Bus NOT used, only PUs

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH GPIO/MISC/NCTF

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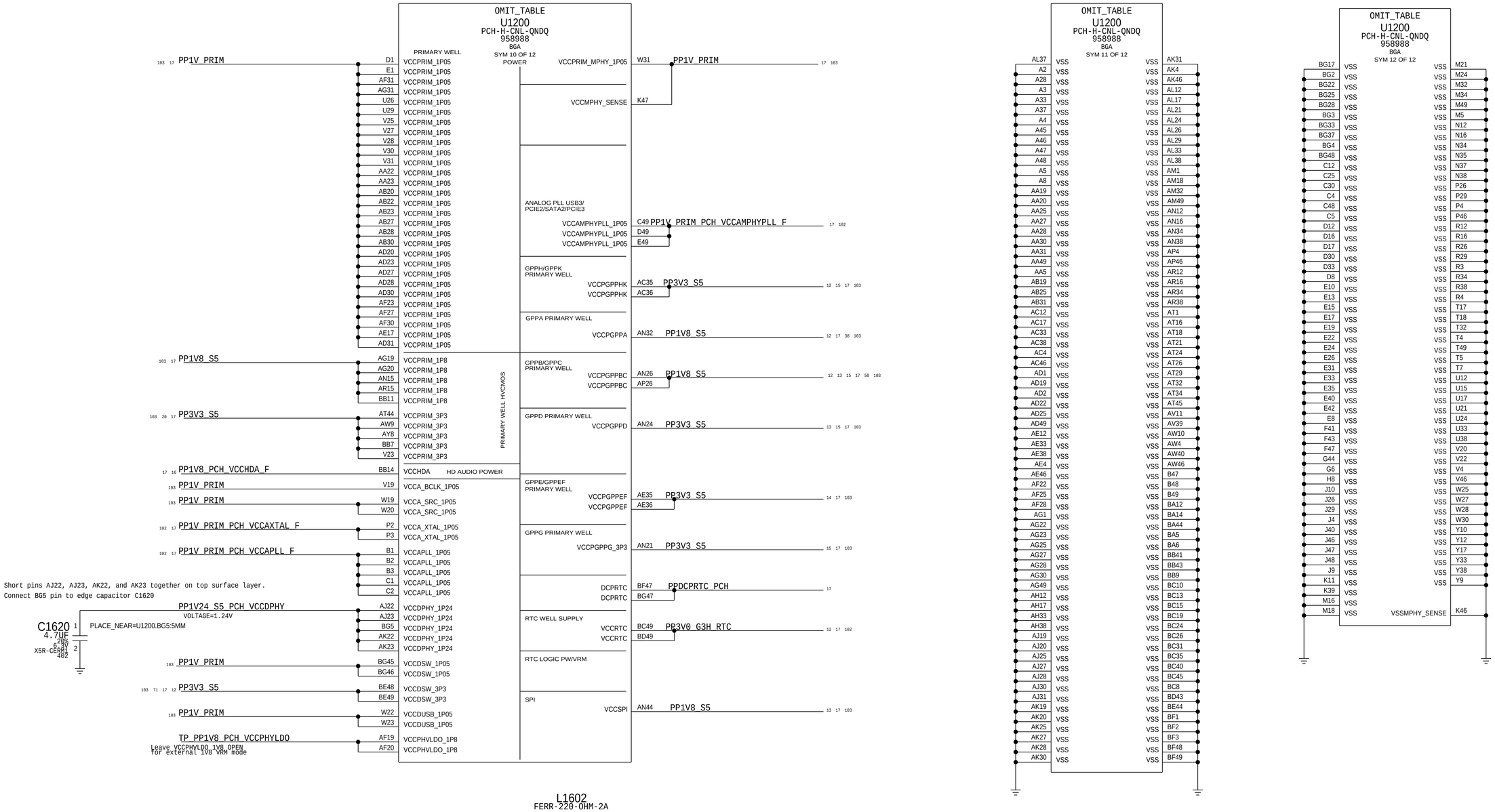

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

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PCH Power

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1000PF CAPS ARE INTEL PLACEHOLDERS & ALL PLACENEAR NEED TO BE UPDATED

PP1V_PRIM
- C1743 1UF 10% 6.3V CERM 402 (PLACE_NEAR=U1200.AF31:3MM)
- C1750 12PF 5% 50V NP0-C0G 0201
- C1730 0.1UF 10% 10V X5R-CERM 0201
- C1731 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.AA23:1.4MM)
- C1732 0.1UF 10% 10V X5R-CERM 0201
- C76 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.U26:5MM)
- C1700 22UF 20% 6.3V X5R-CERM-1 603
- C1701 1UF 10% 6.3V CERM 402 (PLACE_NEAR=U1200.V27:3MM)

PP1V_PRIM
- C1751 12PF 5% 50V NP0-C0G 0201
- C1736 47UF 20% 6.3V POLY-TANT 0805
- C1737 1UF 20% 6.3V X6S-CERM 0201 (PLACE_NEAR=U1200.AD31:2.1MM)
- C1734 0.1UF 10% 10V X5R-CERM 0201
- C1735 0.1UF 10% 10V X5R-CERM 0201
- C1738 1UF 20% 6.3V X6S-CERM 0201
- C1702 1UF 20% 6.3V X6S-CERM 0201 (PLACE_NEAR=U1200.AF31:1MM)

PP1V_PRIM
- C1739 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.AF23:1MM)
- C1703 1UF 20% 6.3V X6S-CERM 0201 (PLACE_NEAR=U1200.V25:1MM)

PPDCPRTC_PCH (VOLTAGE=2.0V)
- C1709 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.BF47:3MM)

PP3V0_G3H_RTC (PLACE_NEAR=U1200.BC49:1MM)
- NOSTUFF C1745 1UF 20% 6.3V X6S-CERM 0201 (PLACE_NEAR=U1200.BC49:1MM)
- NOSTUFF C1715 0.1UF 10% 10V X5R-CERM 0201

Change 1V8_S0_PCH_VCCHDA to 1V8_PCH_VCCHDA_F
Because PCH is using 1V8_PRIM instead of 1V8_S0.

PP1V8_PCH_VCCHDA_F (PLACE_NEAR=U1200.BB14:1.2MM)
- C1749 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.BBI4:1.2MM)
- C1748 22UF 20% 6.3V X5R-CERM-1 603
- C1717 1UF 20% 6.3V X6S-CERM 0201

PP3V3_S5 (PLACE_NEAR=U1200.BB7:3MM)
- C1744 47UF 20% 6.3V POLY-TANT 0805
- C1752 12PF 5% 50V NP0-C0G 0201
- C1719 1UF 20% 6.3V X6S-CERM 0201
- C1720 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.AY8:3MM)

PP3V3_S5
- C1753 12PF 5% 50V NP0-C0G 0201
- C1723 1UF 20% 6.3V X6S-CERM 0201 (PLACE_NEAR=U1200.BE48:1MM)
- C1724 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.BE49:1MM)

PP1V8_S5
- C1757 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.AN44:1MM)

PP1V8_S5
- C1762 1UF 20% 6.3V X6S-CERM 0201 (PLACE_NEAR=U1200.AG19:3MM)

PP1V_PRIM
- C1708 1UF 20% 6.3V X6S-CERM 0201 (PLACE_NEAR=U1200.AB30:1MM)

PP1V8_S5
- C1710 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.AN26:1MM)

PP3V3_S5
- C1713 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.AE35:1MM)

PP1V8_S5
- C1746 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.AN32:1MM)

PP3V3_S5
- C1733 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.AC35:1MM)

PP3V3_S5
- C1747 22UF 20% 6.3V X5R-CERM-1 603 (PLACE_NEAR=U1200.AN21:3MM)
- C1714 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.AN21:3MM)

PP3V3_S5
- C1716 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.AN24:3MM)

PP3V3_S5
- C1718 1UF 20% 6.3V X6S-CERM 0201 (PLACE_NEAR=U1200.BE49:3MM)

PP3V0_G3H_RTC
- C1721 1UF 20% 6.3V X6S-CERM 0201 (PLACE_NEAR=U1200.BD49:3MM)
- C1722 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.BD49:3MM)

RAIL SIDE | PCH SIDE

PP1V_PRIM
- C1754 12PF 5% 50V NP0-C0G 0201
- L1700 2.2UH-20%-0.19A-0.221OHM 0603
- C1704 22UF 20% 6.3V X5R-CERM 0603-1 (PLACE_NEAR=U1200.C49:3MM, PLACE_NEAR=U1200.C49:5MM)
- C1740 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.D49:3MM)
- C1705 1UF 20% 6.3V X6S-CERM 0201 (PLACE_NEAR=U1200.E49:3MM)
- PP1V_PRIM_PCH_VCCAMPHYPLL_F

PP1V_PRIM
- C1755 12PF 5% 50V NP0-C0G 0201
- L1701 2.2UH-20%-0.19A-0.221OHM 0603 (PLACE_NEAR=U1200.P2:1MM)
- C1706 22UF 20% 6.3V X5R-CERM 0603-1 (PLACE_NEAR=U1200.P2:1MM)
- C1741 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.P2:1MM)
- C1707 1UF 20% 6.3V X6S-CERM 0201 (PLACE_NEAR=U1200.P3:1MM)
- PP1V_PRIM_PCH_VCCAXTAL_F

PP1V_PRIM
- C1756 3.0PF +/-0.1PF 50V NP0-C0G 0201
- L1702 2.2UH-20%-0.19A-0.221OHM 0603 (PLACE_NEAR=U1200.B1:5MM)
- C1711 22UF 20% 6.3V X5R-CERM 0603-1 (PLACE_NEAR=U1200.B1:5MM, PLACE_NEAR=U1200.B3:5MM)
- C1742 0.1UF 10% 10V X5R-CERM 0201 (PLACE_NEAR=U1200.C2:5MM)
- C1712 1UF 20% 6.3V X6S-CERM 0201
- PP1V_PRIM_PCH_VCCAPLL_F

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: PCH Decoupling

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 17 OF 142

SHEET: 17 OF 115

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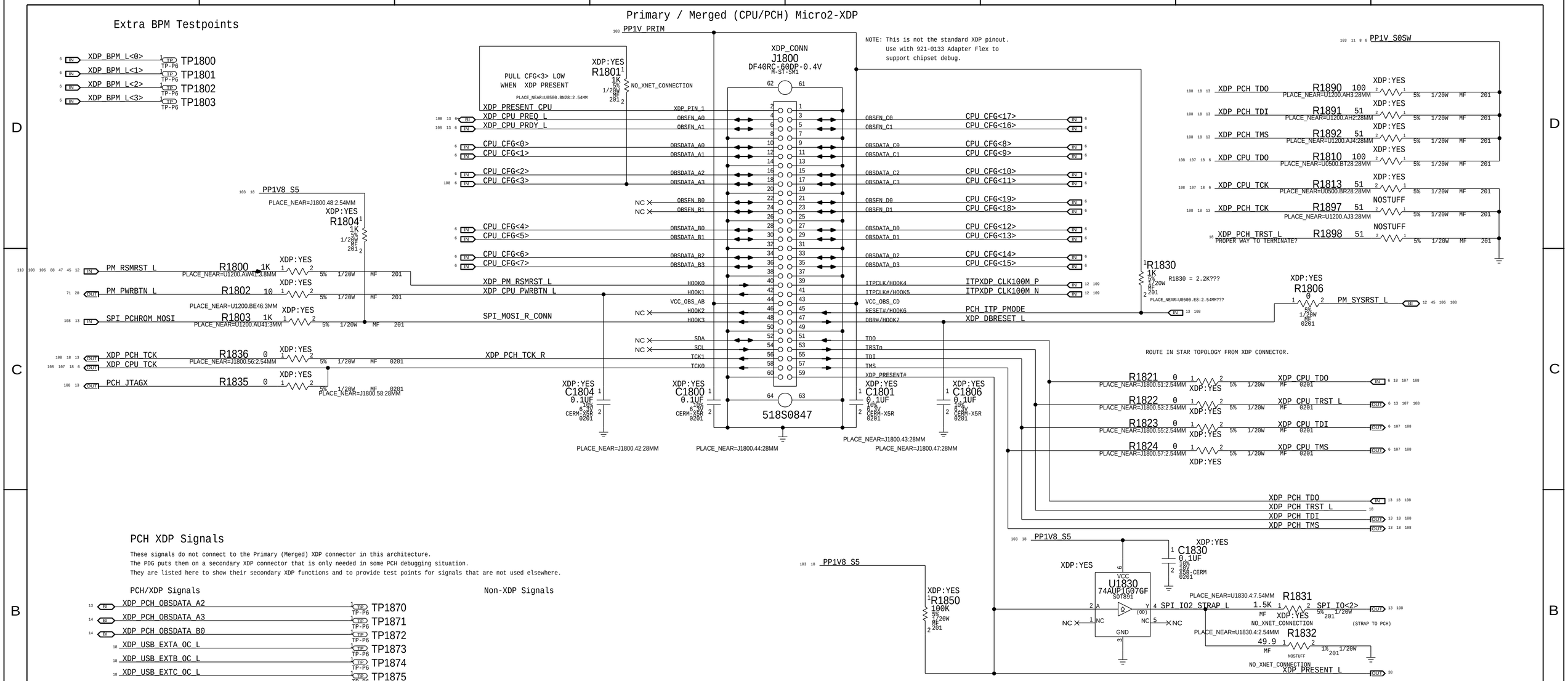

DESIGN: X502/MLB
LAST CHANGE: Mon Jun 15 22:04:28 2015

PAGE TITLE
CPU/PCH Merged XDP

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
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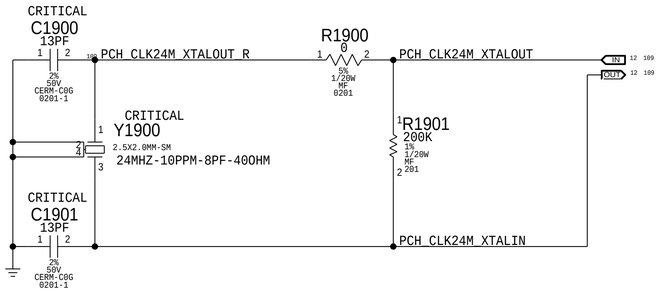
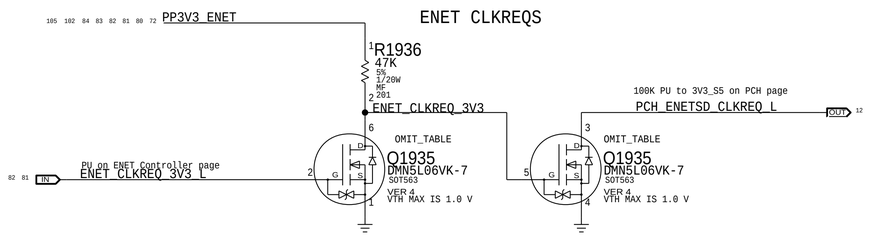
PCH 24MHz Crystal



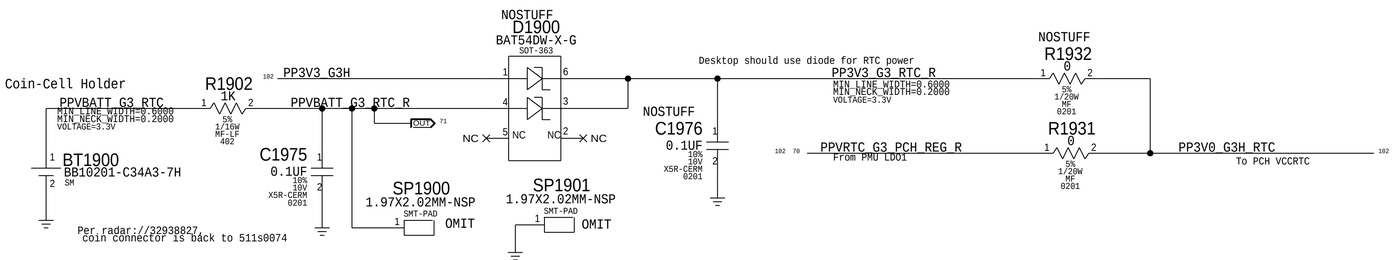
CL (load capacitance) = 8pF
Cs (trace capacitance) = 1pF (assumption)
Ci (package capacitance) = 0.5pF (assumption)
Ce = 2 * (CL - Cs - Ci) = 2 * (8 - 1 -0.5) = 13pF

PDG recommends 18pF,check in charz.

ENET CLKREQS



RTC Power Sources



Per radar://32938827,
coin connector is back to 511s0074

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	Chipset Support 1
	Apple Inc.
DRAWING NUMBER	051-02424
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
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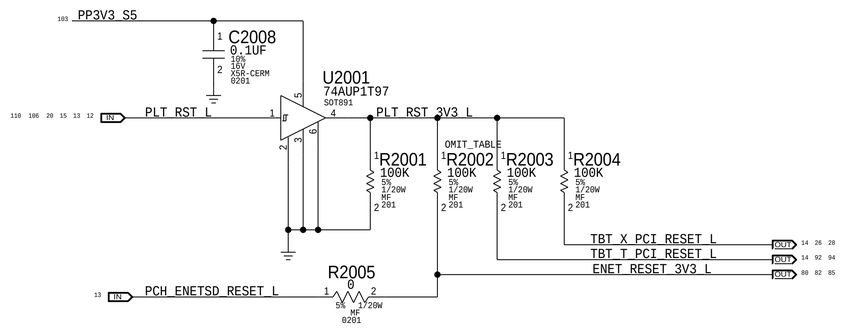
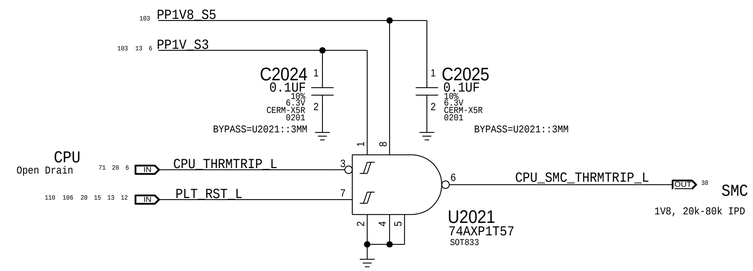
Platform Reset Level Shifter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES, 100K	R2002		ENET:10G
117S0006	1	RES, 1K	R2002		ENET:1G



PMU response will be overridden by SMC, unless SMC and/or PCH is hung.

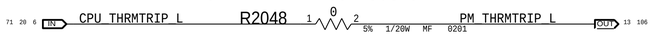
Misc Alias

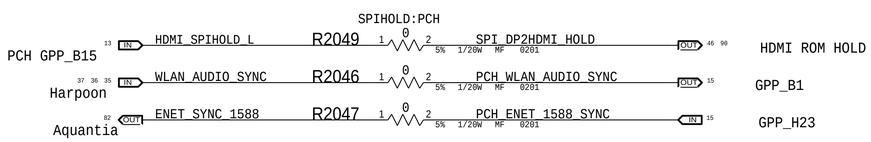
PM_PWRBTN_L	MAKE_BASE=TRUE	PM_PWRBTN_L
PCIE_WLANPCH_D2R_N	MAKE_BASE=TRUE	PCIE_WLANPCH_D2R_N
PCIE_WLANPCH_D2R_P	MAKE_BASE=TRUE	PCIE_WLANPCH_D2R_P
PCIE_WLANPCH_R2D_C_N	MAKE_BASE=TRUE	PCIE_WLANPCH_R2D_C_N
PCIE_WLANPCH_R2D_C_P	MAKE_BASE=TRUE	PCIE_WLANPCH_R2D_C_P
PCIE_WLANPCH_R2D_C_N	MAKE_BASE=TRUE	PCIE_WLANPCH_R2D_C_N
PCIE_WLANPCH_R2D_C_P	MAKE_BASE=TRUE	PCIE_WLANPCH_R2D_C_P
PCIE_CLK100M_WLAN_PCH_N	MAKE_BASE=TRUE	PCIE_CLK100M_WLAN_PCH_N
PCIE_CLK100M_WLAN_PCH_P	MAKE_BASE=TRUE	PCIE_CLK100M_WLAN_PCH_P

PCH NC Pins

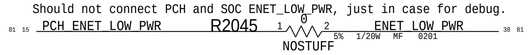
NC_PCH_HSIO_PWR_EN	MAKE_BASE=TRUE	NC_PCH_HSIO_PWR_EN
NC_EDP_BKLT_PWM	MAKE_BASE=TRUE	NC_EDP_BKLT_PWM
NC_PCH_DDPF_CTRLCLK	MAKE_BASE=TRUE	NC_PCH_DDPF_CTRLCLK
NC_PCH_DDPF_CTRLDATA	MAKE_BASE=TRUE	NC_PCH_DDPF_CTRLDATA
NC_PCH_DDPB_CTRLCLK	MAKE_BASE=TRUE	NC_PCH_DDPB_CTRLCLK
NC_PCH_DDPC_CTRLCLK	MAKE_BASE=TRUE	NC_PCH_DDPC_CTRLCLK
NC_PCH_DDPD_CTRLCLK	MAKE_BASE=TRUE	NC_PCH_DDPD_CTRLCLK
NC_TBT_W_PCI_RESET_L	MAKE_BASE=TRUE	NC_TBT_W_PCI_RESET_L
NC_USB_EXTA_HILIM_EN	MAKE_BASE=TRUE	NC_USB_EXTA_HILIM_EN
NC_USB_EXTB_HILIM_EN	MAKE_BASE=TRUE	NC_USB_EXTB_HILIM_EN
NC_USB_EXTC_HILIM_EN	MAKE_BASE=TRUE	NC_USB_EXTC_HILIM_EN
NC_USB_EXTD_HILIM_EN	MAKE_BASE=TRUE	NC_USB_EXTD_HILIM_EN
NC_JTAG_TBT_W_TMS	MAKE_BASE=TRUE	NC_JTAG_TBT_W_TMS
NC_TBT_W_PLUG_EVENT_L	MAKE_BASE=TRUE	NC_TBT_W_PLUG_EVENT_L
NC_PCH_BSSB_CLK	MAKE_BASE=TRUE	NC_PCH_BSSB_CLK
NC_PCH_BSSB_DATA	MAKE_BASE=TRUE	NC_PCH_BSSB_DATA
NC_PCH_I2C_UPC_SDA	MAKE_BASE=TRUE	NC_PCH_I2C_UPC_SDA
NC_PCH_I2C_UPC_SCL	MAKE_BASE=TRUE	NC_PCH_I2C_UPC_SCL
NC_PCH_I2C_UPC_INT_L	MAKE_BASE=TRUE	NC_PCH_I2C_UPC_INT_L

PCH THRMTRIP connection

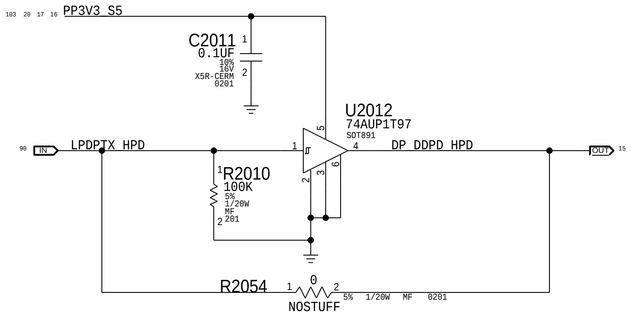




Should not connect PCH and SOC ENET_LOW_PWR, just in case for debug.



HDMI HPD



Display Port DDPB, DDPC,DDPD

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
Chipset Support 2

Apple Inc.

DRAWING NUMBER 051-02424 | SIZE D
REVISION 6.0.0
BRANCH dvt-1
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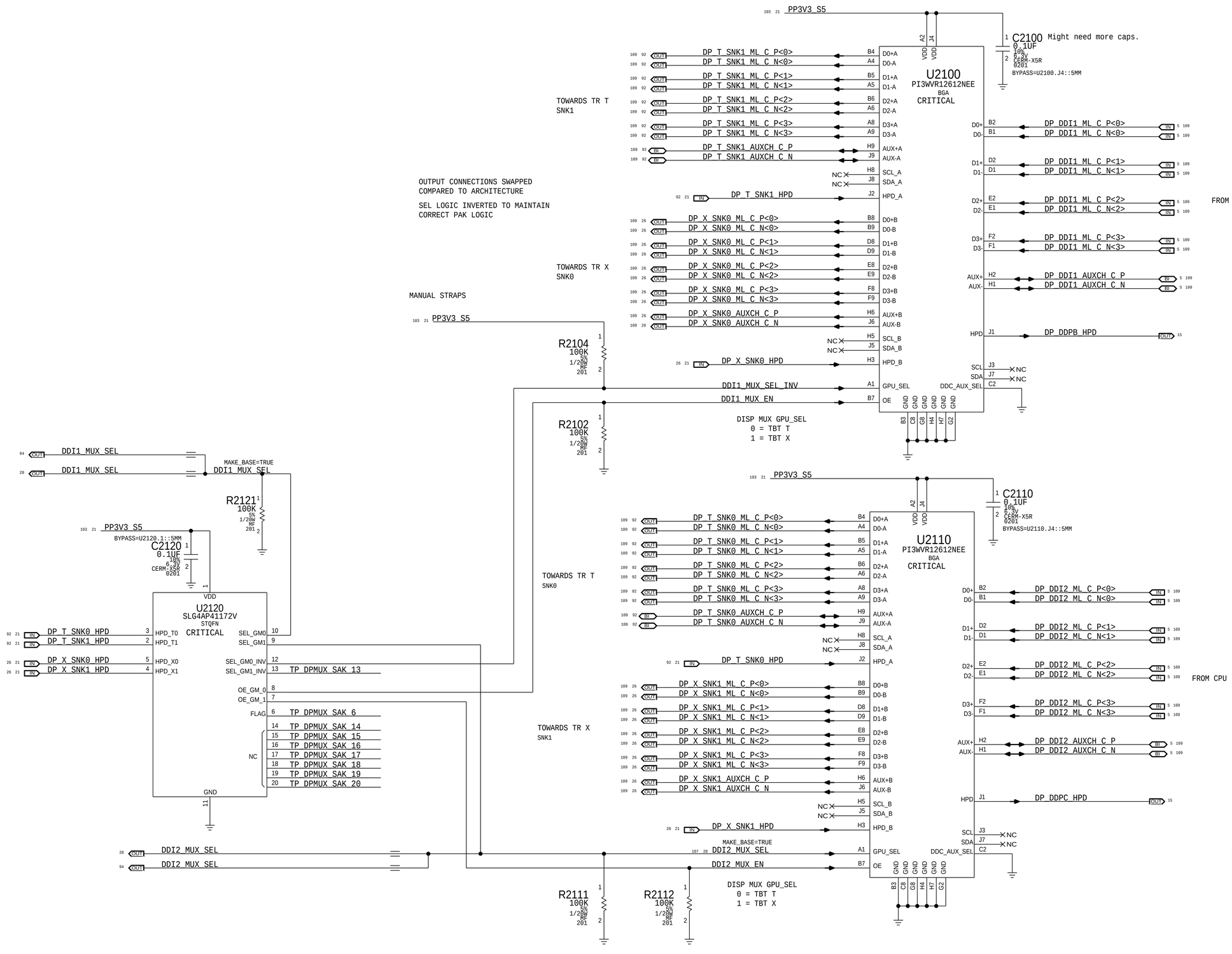

PAGE TITLE

Display Mux

Apple Inc.

DRAWING NUMBER 051-02424 | SIZE D

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BRANCH dvt-1

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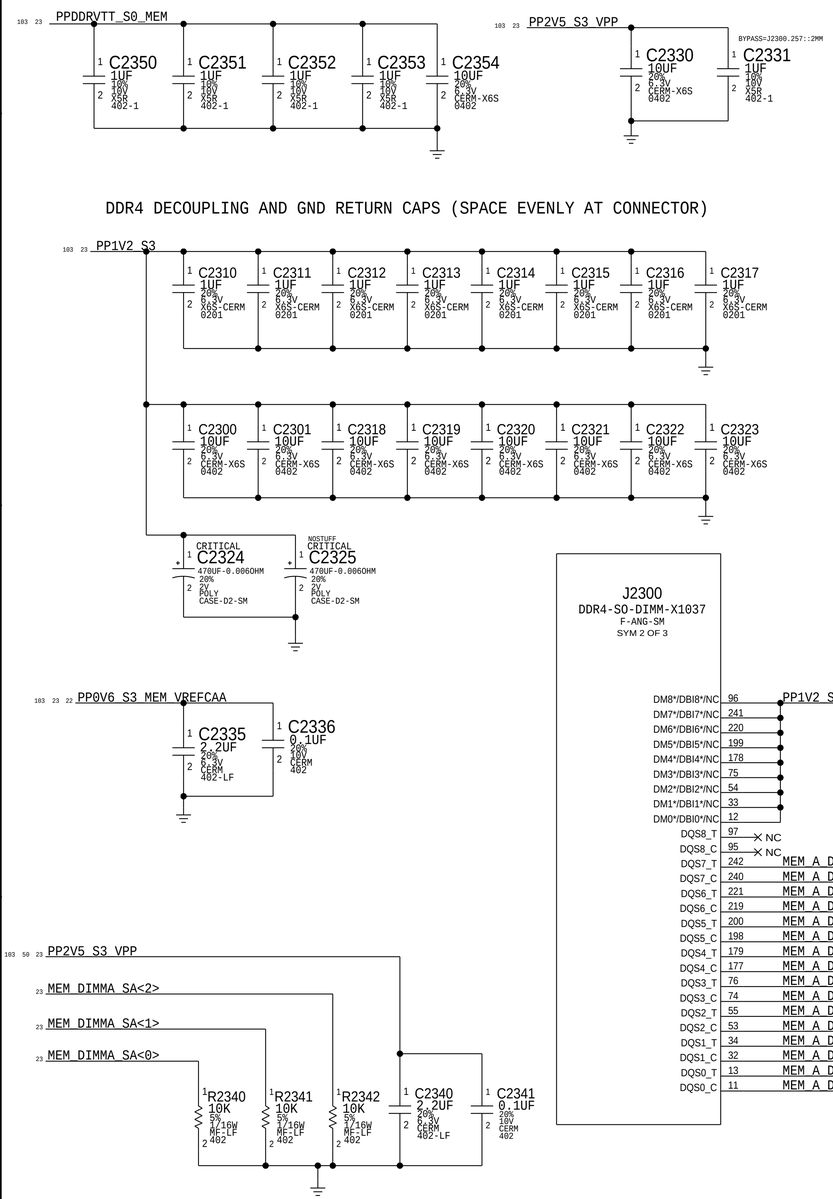
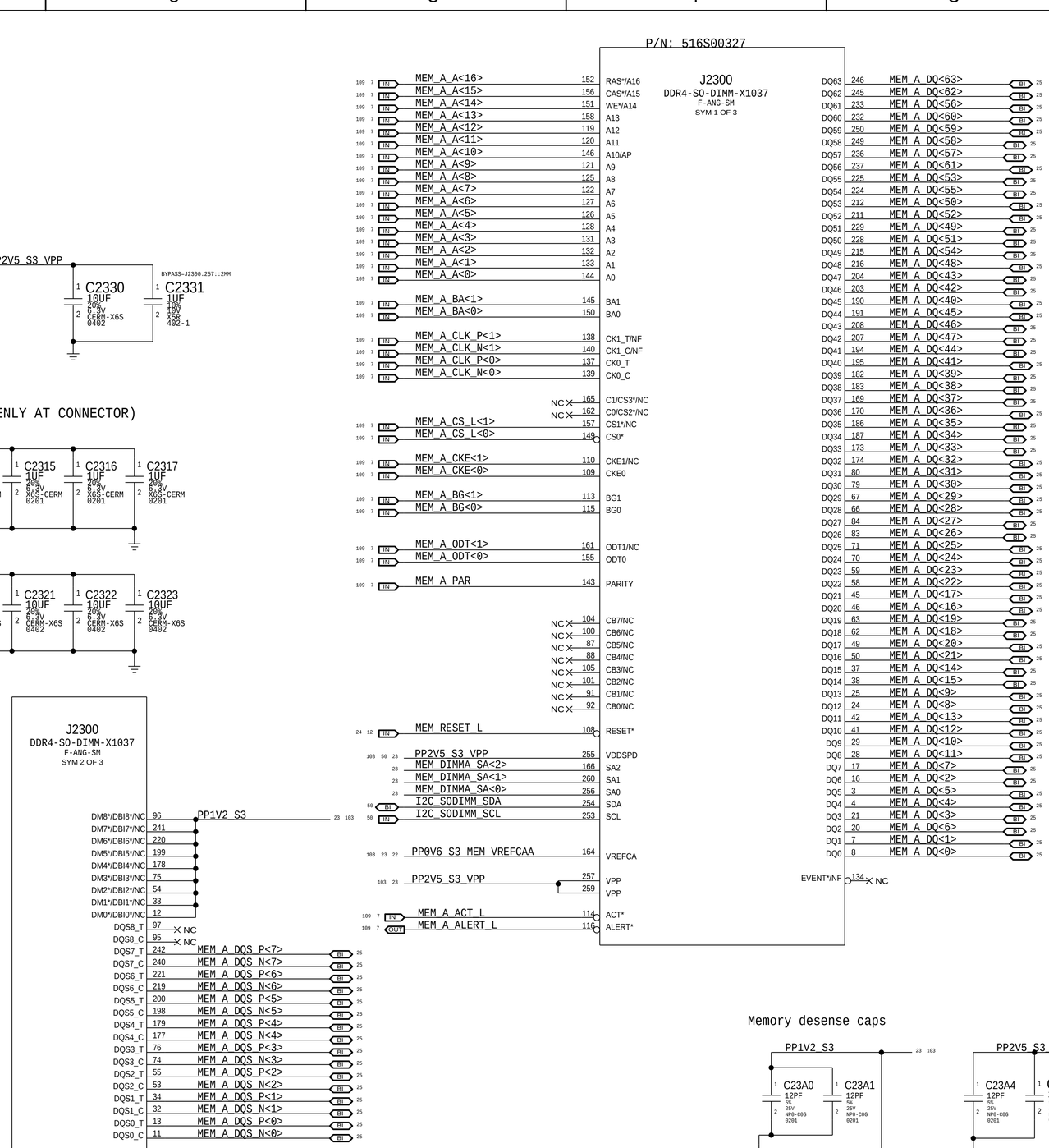
Page Notes

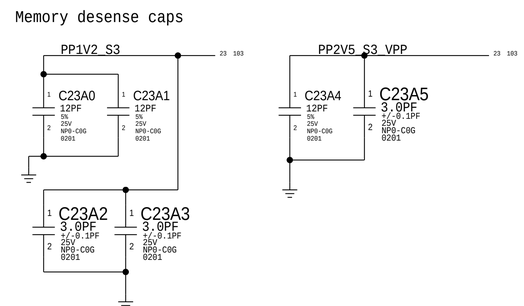
Power aliases required by this page:
- =PPDDRVPP_S3_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PP2V5_S3_MEM_A_SPD (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
{NONE}







BOM_COST_GROUP=DRAM

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: DDR4 DIM A

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 23 OF 142

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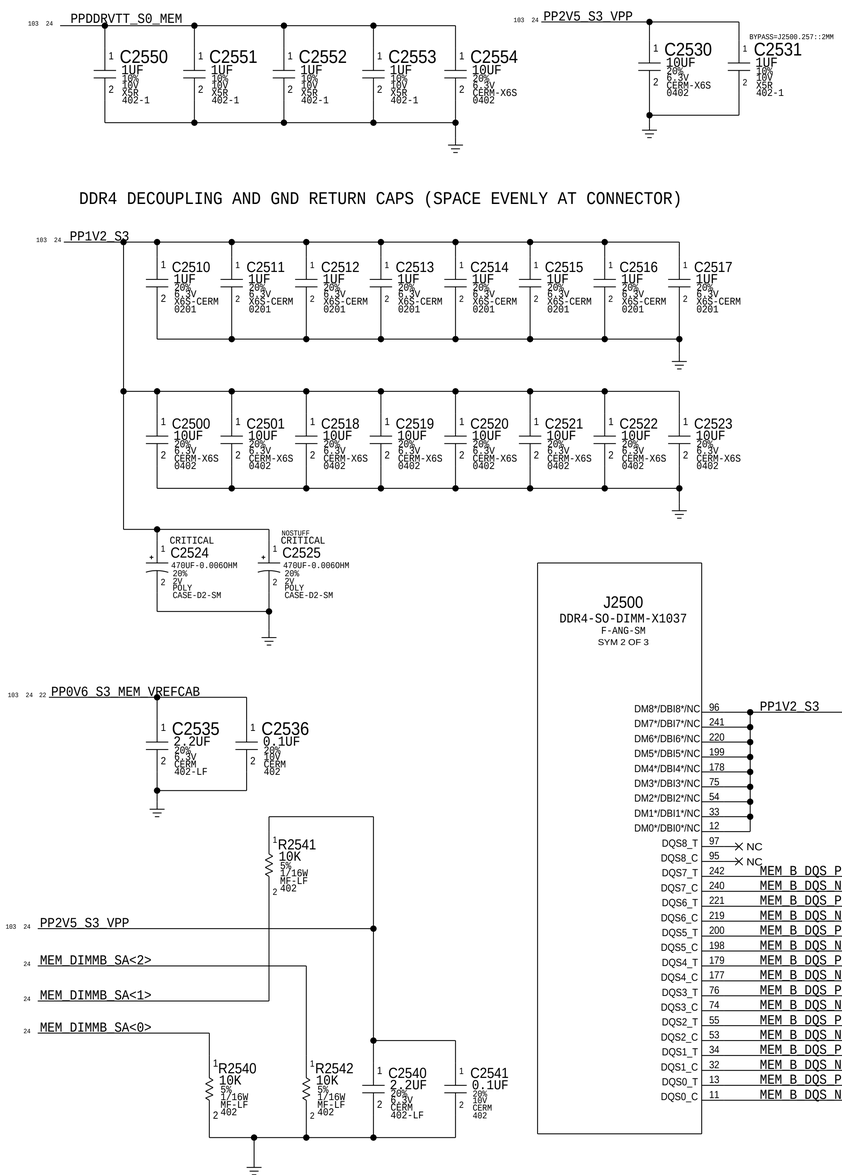
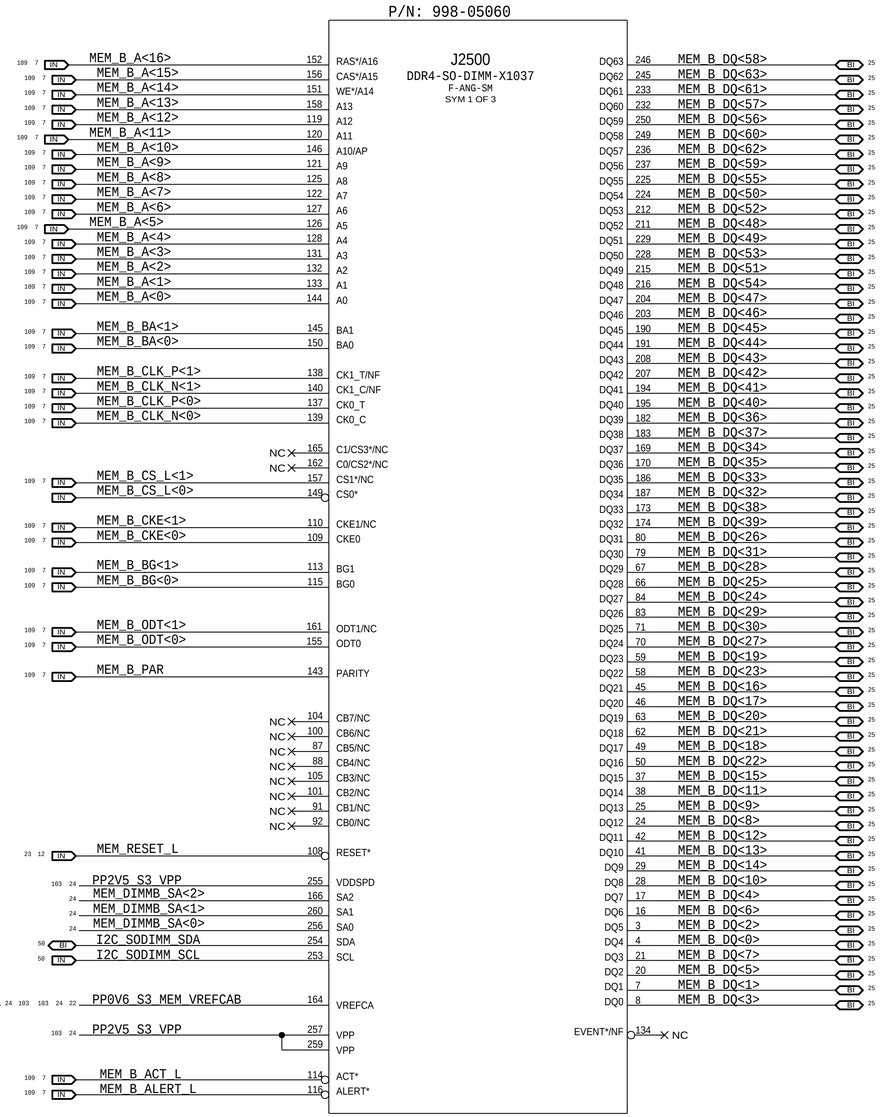
Page Notes

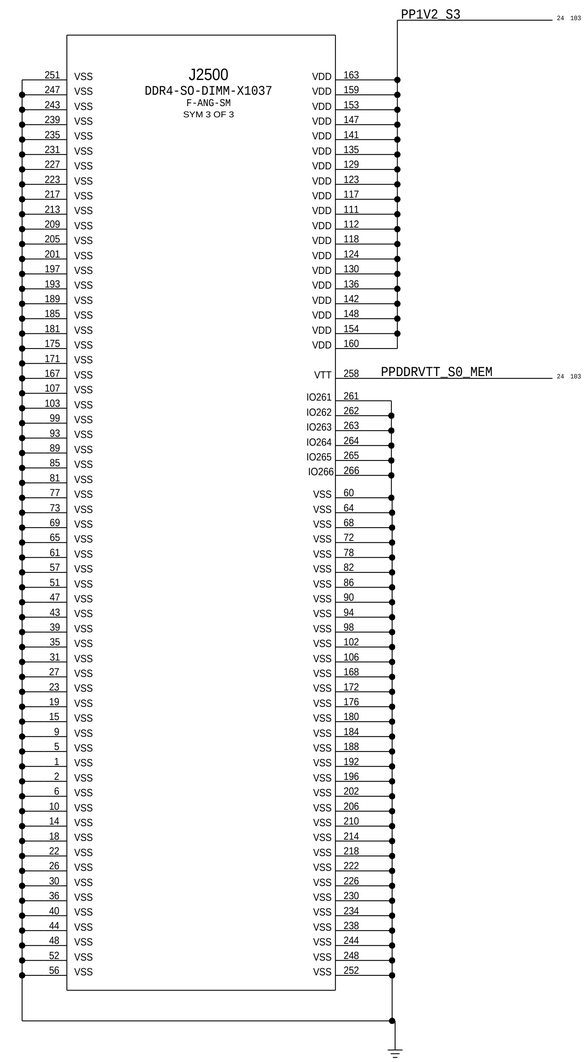
Power aliases required by this page:
- =PPDDRVPP_S3_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PP2V5_S3_MEM_B_SPD (2.5 - 3.3V)

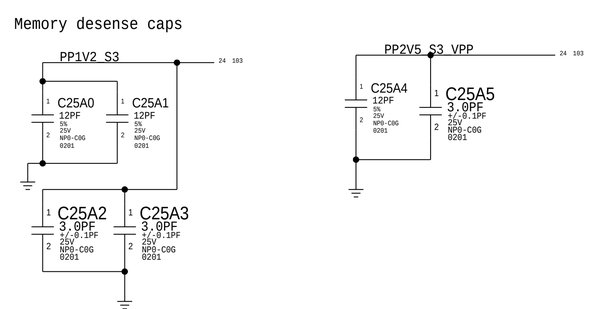
Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)









BOM_COST_GROUP=DRAM

SYNC_MASTER=Mary	SYNC_DATE=04/26/2018
PAGE TITLE: DDR4 DIM B	
Apple Inc.	DRAWING NUMBER: 051-02424 SIZE: D
	REVISION: 6.0.0
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Memory Bit/Byte Swizzle

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	MEM_A_DQS_N<0>	MEM_B_DQS_N<0>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	MEM_A_DQS_P<0>	MEM_B_DQS_P<0>
MEM_A_DQ<7>	MAKE_BASE=TRUE	MEM_A_DQ<7>	MEM_B_DQ<4>
MEM_A_DQ<2>	MAKE_BASE=TRUE	MEM_A_DQ<2>	MEM_B_DQ<6>
MEM_A_DQ<5>	MAKE_BASE=TRUE	MEM_A_DQ<5>	MEM_B_DQ<2>
MEM_A_DQ<4>	MAKE_BASE=TRUE	MEM_A_DQ<4>	MEM_B_DQ<0>
MEM_A_DQ<3>	MAKE_BASE=TRUE	MEM_A_DQ<3>	MEM_B_DQ<7>
MEM_A_DQ<6>	MAKE_BASE=TRUE	MEM_A_DQ<6>	MEM_B_DQ<5>
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MEM_A_DQS_N<1>	MAKE_BASE=TRUE	MEM_A_DQS_N<1>	MEM_B_DQS_N<1>
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MEM_A_DQ<12>	MAKE_BASE=TRUE	MEM_A_DQ<12>	MEM_B_DQ<13>
MEM_A_DQ<10>	MAKE_BASE=TRUE	MEM_A_DQ<10>	MEM_B_DQ<14>
MEM_A_DQ<11>	MAKE_BASE=TRUE	MEM_A_DQ<11>	MEM_B_DQ<10>
MEM_A_DQS_N<2>	MAKE_BASE=TRUE	MEM_A_DQS_N<2>	MEM_B_DQS_N<2>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	MEM_A_DQS_P<2>	MEM_B_DQS_P<2>
MEM_A_DQ<23>	MAKE_BASE=TRUE	MEM_A_DQ<23>	MEM_B_DQ<19>
MEM_A_DQ<22>	MAKE_BASE=TRUE	MEM_A_DQ<22>	MEM_B_DQ<23>
MEM_A_DQ<17>	MAKE_BASE=TRUE	MEM_A_DQ<17>	MEM_B_DQ<16>
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MEM_A_DQ<19>	MAKE_BASE=TRUE	MEM_A_DQ<19>	MEM_B_DQ<20>
MEM_A_DQ<18>	MAKE_BASE=TRUE	MEM_A_DQ<18>	MEM_B_DQ<21>
MEM_A_DQ<20>	MAKE_BASE=TRUE	MEM_A_DQ<20>	MEM_B_DQ<18>
MEM_A_DQ<21>	MAKE_BASE=TRUE	MEM_A_DQ<21>	MEM_B_DQ<22>
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MEM_A_DQS_P<3>	MAKE_BASE=TRUE	MEM_A_DQS_P<3>	MEM_B_DQS_P<3>
MEM_A_DQ<31>	MAKE_BASE=TRUE	MEM_A_DQ<31>	MEM_B_DQ<26>
MEM_A_DQ<30>	MAKE_BASE=TRUE	MEM_A_DQ<30>	MEM_B_DQ<31>
MEM_A_DQ<29>	MAKE_BASE=TRUE	MEM_A_DQ<29>	MEM_B_DQ<28>
MEM_A_DQ<28>	MAKE_BASE=TRUE	MEM_A_DQ<28>	MEM_B_DQ<25>
MEM_A_DQ<27>	MAKE_BASE=TRUE	MEM_A_DQ<27>	MEM_B_DQ<24>
MEM_A_DQ<26>	MAKE_BASE=TRUE	MEM_A_DQ<26>	MEM_B_DQ<29>
MEM_A_DQ<25>	MAKE_BASE=TRUE	MEM_A_DQ<25>	MEM_B_DQ<30>
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MEM_A_DQS_P<4>	MAKE_BASE=TRUE	MEM_A_DQS_P<4>	MEM_B_DQS_P<4>
MEM_A_DQ<39>	MAKE_BASE=TRUE	MEM_A_DQ<39>	MEM_B_DQ<36>
MEM_A_DQ<38>	MAKE_BASE=TRUE	MEM_A_DQ<38>	MEM_B_DQ<37>
MEM_A_DQ<37>	MAKE_BASE=TRUE	MEM_A_DQ<37>	MEM_B_DQ<34>
MEM_A_DQ<36>	MAKE_BASE=TRUE	MEM_A_DQ<36>	MEM_B_DQ<35>
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MEM_A_DQ<34>	MAKE_BASE=TRUE	MEM_A_DQ<34>	MEM_B_DQ<32>
MEM_A_DQ<33>	MAKE_BASE=TRUE	MEM_A_DQ<33>	MEM_B_DQ<38>
MEM_A_DQ<32>	MAKE_BASE=TRUE	MEM_A_DQ<32>	MEM_B_DQ<39>
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MEM_A_DQS_P<5>	MAKE_BASE=TRUE	MEM_A_DQS_P<5>	MEM_B_DQS_P<5>
MEM_A_DQ<43>	MAKE_BASE=TRUE	MEM_A_DQ<43>	MEM_B_DQ<47>
MEM_A_DQ<42>	MAKE_BASE=TRUE	MEM_A_DQ<42>	MEM_B_DQ<46>
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MEM_A_DQ<45>	MAKE_BASE=TRUE	MEM_A_DQ<45>	MEM_B_DQ<44>
MEM_A_DQ<46>	MAKE_BASE=TRUE	MEM_A_DQ<46>	MEM_B_DQ<43>
MEM_A_DQ<47>	MAKE_BASE=TRUE	MEM_A_DQ<47>	MEM_B_DQ<42>
MEM_A_DQ<44>	MAKE_BASE=TRUE	MEM_A_DQ<44>	MEM_B_DQ<41>
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MEM_A_DQS_P<6>	MAKE_BASE=TRUE	MEM_A_DQS_P<6>	MEM_B_DQS_P<6>
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MEM_A_DQ<55>	MAKE_BASE=TRUE	MEM_A_DQ<55>	MEM_B_DQ<50>
MEM_A_DQ<50>	MAKE_BASE=TRUE	MEM_A_DQ<50>	MEM_B_DQ<52>
MEM_A_DQ<52>	MAKE_BASE=TRUE	MEM_A_DQ<52>	MEM_B_DQ<48>
MEM_A_DQ<49>	MAKE_BASE=TRUE	MEM_A_DQ<49>	MEM_B_DQ<49>
MEM_A_DQ<51>	MAKE_BASE=TRUE	MEM_A_DQ<51>	MEM_B_DQ<53>
MEM_A_DQ<54>	MAKE_BASE=TRUE	MEM_A_DQ<54>	MEM_B_DQ<51>
MEM_A_DQ<48>	MAKE_BASE=TRUE	MEM_A_DQ<48>	MEM_B_DQ<54>
MEM_A_DQS_N<7>	MAKE_BASE=TRUE	MEM_A_DQS_N<7>	MEM_B_DQS_N<7>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	MEM_A_DQS_P<7>	MEM_B_DQS_P<7>
MEM_A_DQ<63>	MAKE_BASE=TRUE	MEM_A_DQ<63>	MEM_B_DQ<58>
MEM_A_DQ<62>	MAKE_BASE=TRUE	MEM_A_DQ<62>	MEM_B_DQ<63>
MEM_A_DQ<56>	MAKE_BASE=TRUE	MEM_A_DQ<56>	MEM_B_DQ<61>
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MEM_A_DQ<61>	MAKE_BASE=TRUE	MEM_A_DQ<61>	MEM_B_DQ<59>

BOM_COST_GROUP=DRAM

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
DRAM: ALIASES AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

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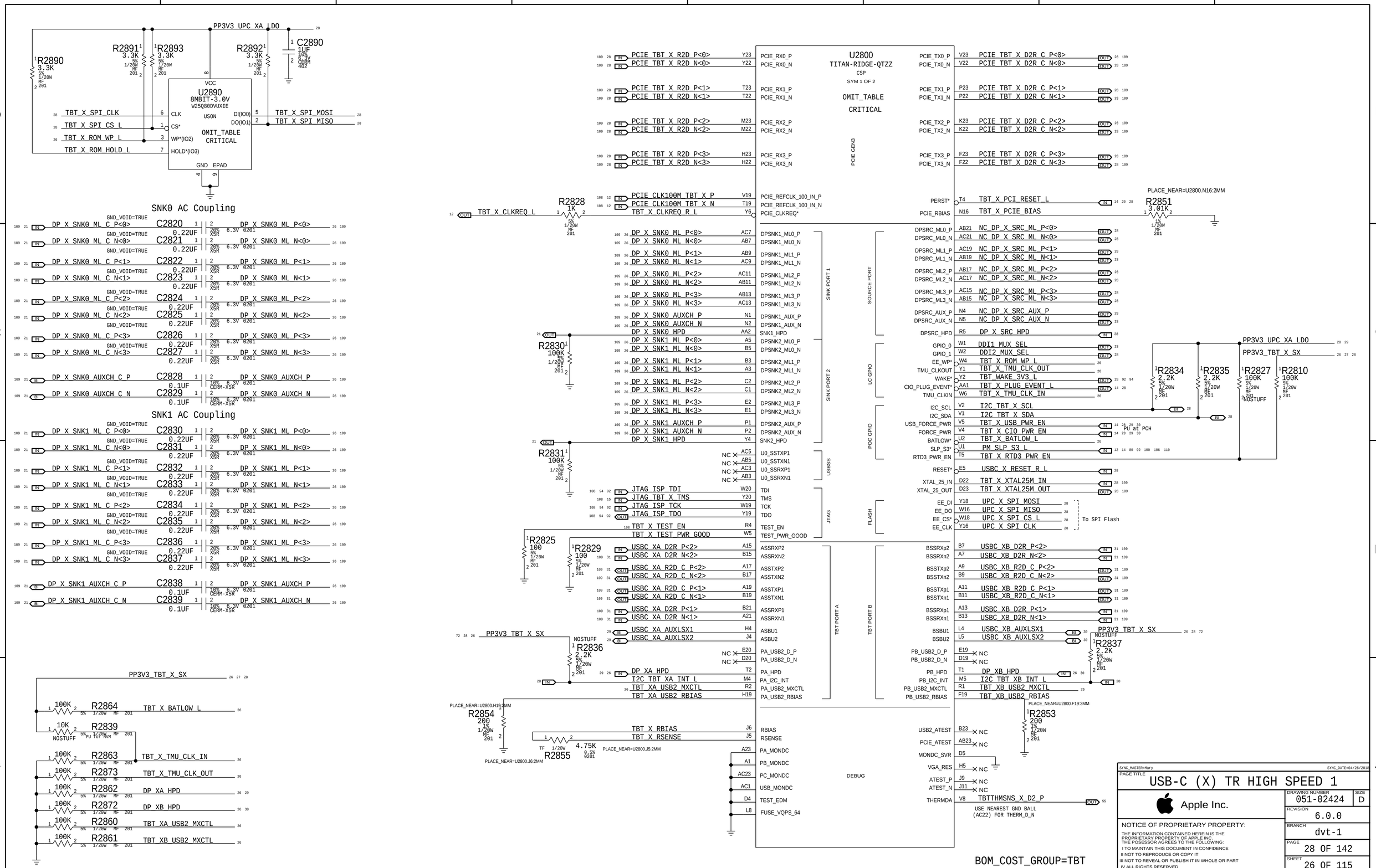
PP3V3_UPC_XA_LDO
R2890 3.3K
R2891 3.3K
R2893 3.3K
R2892 3.3K
C2890 1UF
U2890 8MBIT-3.0V W25Q80DVUXIE USON
OMIT_TABLE CRITICAL
TBT_X_SPI_CLK
TBT_X_SPI_CS_L
TBT_X_ROM_WP_L
TBT_X_ROM_HOLD_L
TBT_X_SPI_MOSI
TBT_X_SPI_MISO
SNK0 AC Coupling
SNK1 AC Coupling
U2800 TITAN-RIDGE-QTZZ CSP SYM 1 OF 2
OMIT_TABLE CRITICAL
PCIE GEN3
SINK PORT 1
SINK PORT 2
SOURCE PORT
LC GPIO
POC GPIO
USB5S5
JTAG
FLASH
TBT PORT A
TBT PORT B
DEBUG
TBT_X_CLKREQ_L
R2828 1K
R2830 100K
R2831 100K
R2825 100
R2829 100
R2836 2.2K
R2854 200
R2855 4.75K
R2851 3.01K
R2834 2.2K
R2835 2.2K
R2827 100K
R2810 100K
R2837 2.2K
R2853 200
PP3V3_TBT_X_SX
R2864 100K
R2839 10K
R2863 100K
R2873 100K
R2862 100K
R2872 100K
R2860 100K
R2861 100K
BOM_COST_GROUP=TBT
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
USB-C (X) TR HIGH SPEED 1
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
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SHEET 26 OF 115
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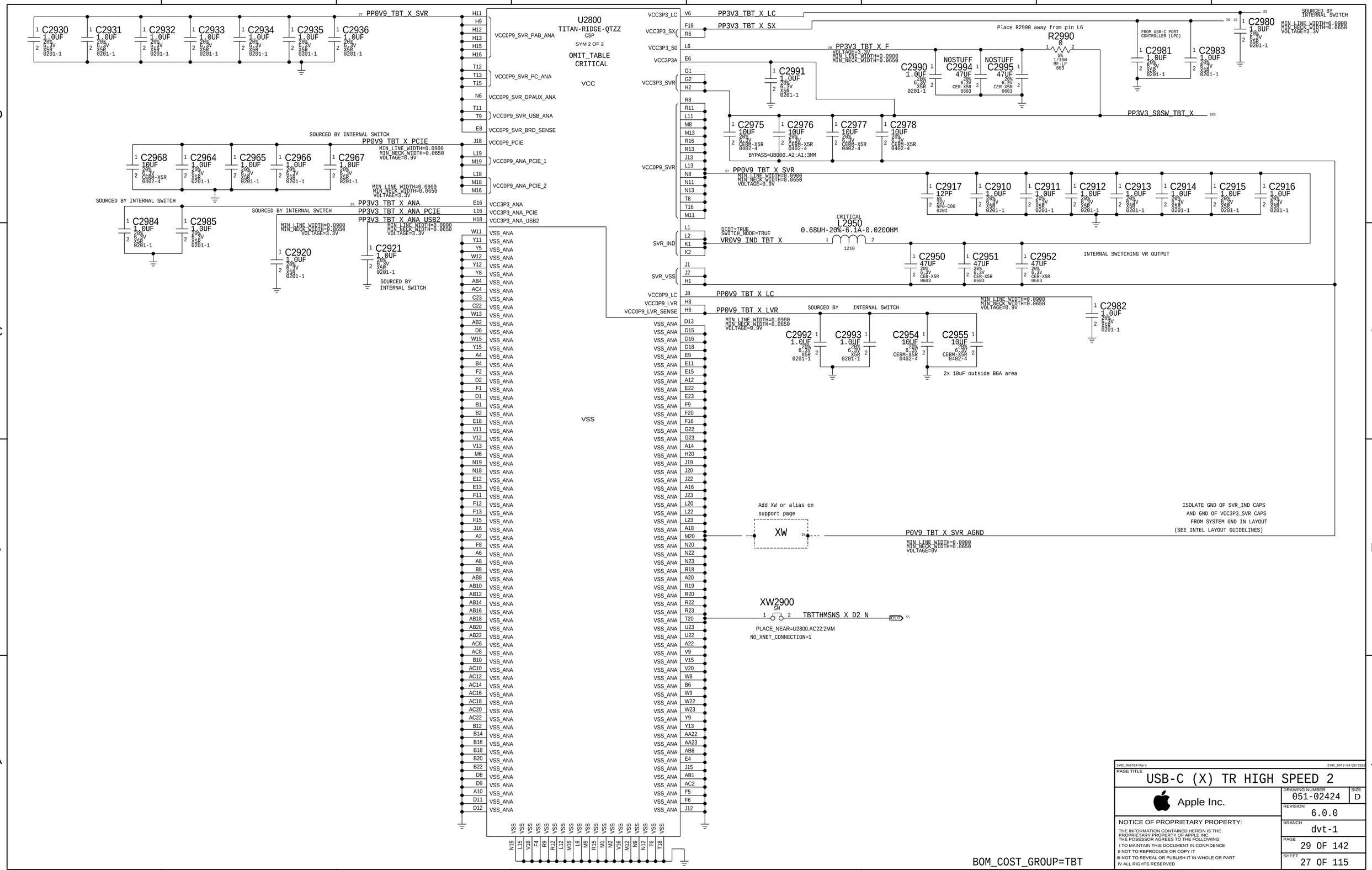

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
USB-C (X) TR HIGH SPEED 2

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

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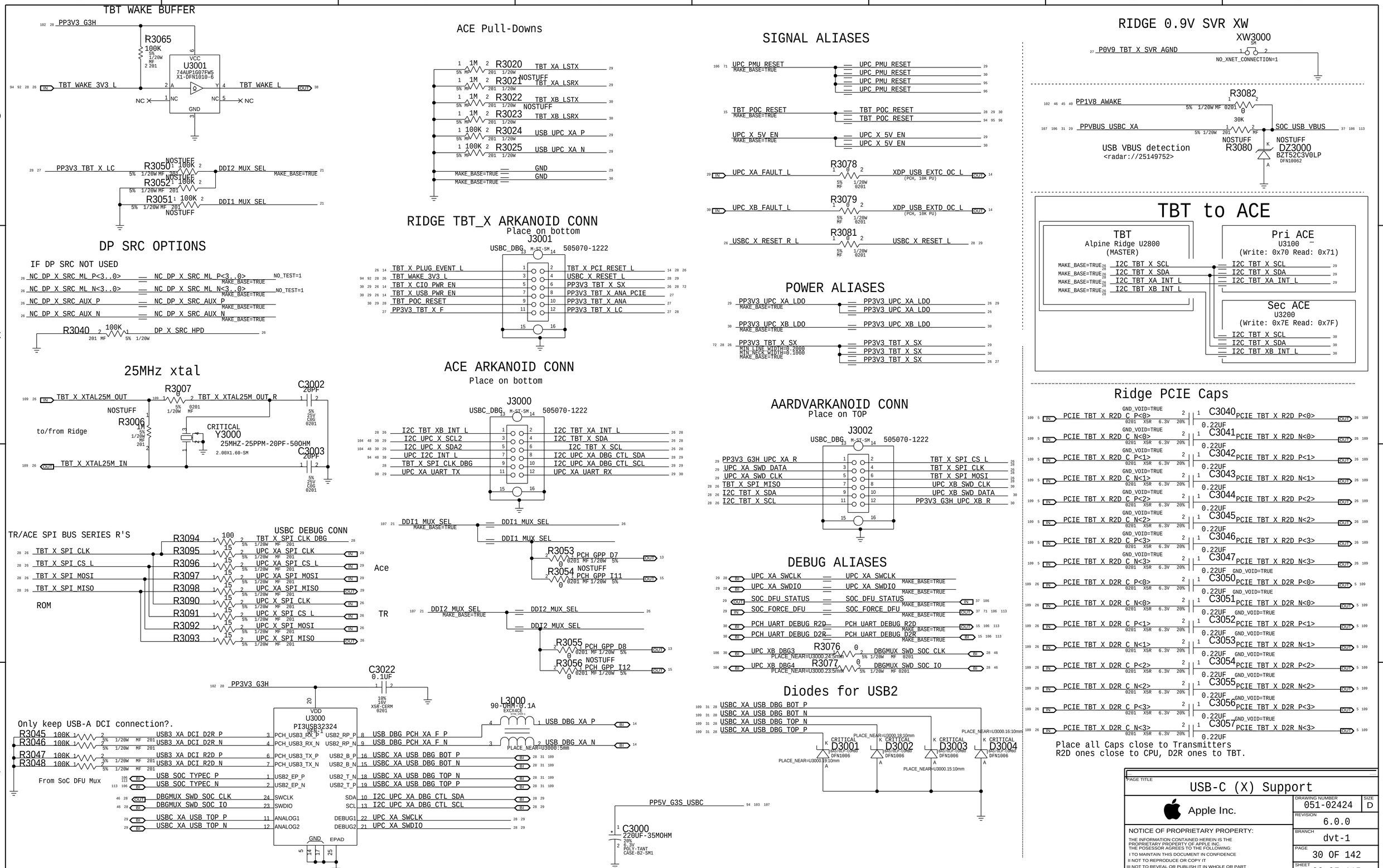
TBT WAKE BUFFER
PP3V3_G3H
R3065
100K
TBT_WAKE_3V3_L
U3001
74AUP1G07FW5
X1-DFN1010-6
TBT_WAKE_L
NC
GND
PP3V3_TBT_X_LC
R3050 100K NOSTUFF
R3052 100K NOSTUFF
R3051 100K NOSTUFF
DDI2_MUX_SEL
DDI1_MUX_SEL
DP SRC OPTIONS
IF DP SRC NOT USED
NC_DP_X_SRC_ML_P<3..0>
NC_DP_X_SRC_ML_N<3..0>
NC_DP_X_SRC_AUX_P
NC_DP_X_SRC_AUX_N
NO_TEST=1
MAKE_BASE=TRUE
R3040 100K
DP_X_SRC_HPD
25MHz xtal
TBT_X_XTAL25M_OUT
R3007 0
TBT_X_XTAL25M_OUT_R
C3002 20PF
R3006 1M NOSTUFF
CRITICAL
Y3000
25MHZ-25PPM-20PF-50OHM
2.00X1.60-SM
C3003 20PF
to/from Ridge
TBT_X_XTAL25M_IN
ACE Pull-Downs
R3020 1M TBT_XA_LSTX
R3021 1M NOSTUFF TBT_XA_LSRX
R3022 1M TBT_XB_LSTX NOSTUFF
R3023 1M TBT_XB_LSRX
R3024 100K USB_UPC_XA_P
R3025 100K USB_UPC_XA_N
GND
RIDGE TBT_X ARKANOID CONN
Place on bottom
J3001
USBC_DBG
505070-1222
TBT_X_PLUG_EVENT_L
TBT_WAKE_3V3_L
TBT_X_CIO_PWR_EN
TBT_X_USB_PWR_EN
TBT_POC_RESET
PP3V3_TBT_X_F
TBT_X_PCI_RESET_L
USBC_X_RESET_L
PP3V3_TBT_X_SX
PP3V3_TBT_X_ANA_PCIE
PP3V3_TBT_X_ANA
PP3V3_TBT_X_LC
ACE ARKANOID CONN
Place on bottom
J3000
I2C_TBT_XB_INT_L
I2C_UPC_X_SCL2
I2C_UPC_X_SDA2
UPC_I2C_INT_L
TBT_X_SPI_CLK_DBG
UPC_XA_UART_TX
I2C_TBT_XA_INT_L
I2C_TBT_X_SDA
I2C_TBT_X_SCL
I2C_UPC_XA_DBG_CTL_SDA
I2C_UPC_XA_DBG_CTL_SCL
UPC_XA_UART_RX
DDI1_MUX_SEL
R3053 0 PCH_GPP_D7
R3054 0 NOSTUFF PCH_GPP_I11
Ace
TR
DDI2_MUX_SEL
R3055 0 PCH_GPP_D8
R3056 0 NOSTUFF PCH_GPP_I12
TR/ACE SPI BUS SERIES R'S
TBT_X_SPI_CLK
TBT_X_SPI_CS_L
TBT_X_SPI_MOSI
TBT_X_SPI_MISO
R3094 100
R3095 15
R3096 15
R3097 15
R3098 15
R3090 15
R3091 15
R3092 15
R3093 15
TBT_X_SPI_CLK_DBG
UPC_XA_SPI_CLK
UPC_XA_SPI_CS_L
UPC_XA_SPI_MOSI
UPC_XA_SPI_MISO
UPC_X_SPI_CLK
UPC_X_SPI_CS_L
UPC_X_SPI_MOSI
UPC_X_SPI_MISO
ROM
USBC DEBUG CONN
C3022 0.1UF
PP3V3_G3H
U3000
PI3USB32324
VDD
GND
EPAD
Only keep USB-A DCI connection?.
R3045 100K USB3_XA_DCI_D2R_P
R3046 100K USB3_XA_DCI_D2R_N
R3047 100K USB3_XA_DCI_R2D_P
R3048 100K USB3_XA_DCI_R2D_N
From SoC DFU Mux
USB_SOC_TYPEC_P
USB_SOC_TYPEC_N
DBGMUX_SWD_SOC_CLK
DBGMUX_SWD_SOC_IO
USBC_XA_USB_TOP_P
USBC_XA_USB_TOP_N
PCH_USB3_RX_P
PCH_USB3_RX_N
PCH_USB3_TX_P
PCH_USB3_TX_N
USB2_EP_P
USB2_EP_N
SWCLK
SWDIO
ANALOG1
ANALOG2
USB2_RP_P
USB2_RP_N
USB2_B_P
USB2_B_N
USB2_T_N
USB2_T_P
SDA
SCL
DEBUG1
DEBUG2
USB_DBG_PCH_XA_F_P
USB_DBG_PCH_XA_F_N
USBC_XA_USB_DBG_BOT_P
USBC_XA_USB_DBG_BOT_N
USBC_XA_USB_DBG_TOP_N
USBC_XA_USB_DBG_TOP_P
I2C_UPC_XA_DBG_CTL_SDA
I2C_UPC_XA_DBG_CTL_SCL
UPC_XA_SWCLK
UPC_XA_SWDIO
L3000
90-OHM-0.1A
EXC44CE
USB_DBG_XA_P
USB_DBG_XA_N
PLACE_NEAR=U3000:5mm
PP5V_G3S_USBC
C3000 220UF-35MOHM
POLY-TANT
CASE-B2-SM1
SIGNAL ALIASES
UPC_PMU_RESET
TBT_POC_RESET
UPC_X_5V_EN
UPC_XA_FAULT_L
UPC_XB_FAULT_L
USBC_X_RESET_R_L
R3078 0 XDP_USB_EXTC_OC_L
R3079 0 XDP_USB_EXTD_OC_L
R3081 0 USBC_X_RESET_L
(PCH, 10K PU)
POWER ALIASES
PP3V3_UPC_XA_LDO
PP3V3_UPC_XB_LDO
PP3V3_TBT_X_SX
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
AARDVARKANOID CONN
Place on TOP
J3002
PP3V3_G3H_UPC_XA_R
UPC_XA_SWD_DATA
UPC_XA_SWD_CLK
TBT_X_SPI_MISO
I2C_TBT_X_SDA
I2C_TBT_X_SCL
TBT_X_SPI_CS_L
TBT_X_SPI_CLK
TBT_X_SPI_MOSI
UPC_XB_SWD_CLK
UPC_XB_SWD_DATA
PP3V3_G3H_UPC_XB_R
DEBUG ALIASES
UPC_XA_SWCLK
UPC_XA_SWDIO
SOC_DFU_STATUS
SOC_FORCE_DFU
PCH_UART_DEBUG_R2D
PCH_UART_DEBUG_D2R
UPC_XB_DBG3
UPC_XB_DBG4
R3076 0 DBGMUX_SWD_SOC_CLK
R3077 0 DBGMUX_SWD_SOC_IO
PLACE_NEAR=U3000:24.5mm
PLACE_NEAR=U3000:23.5mm
Diodes for USB2
USBC_XA_USB_DBG_BOT_P
USBC_XA_USB_DBG_BOT_N
USBC_XA_USB_DBG_TOP_N
USBC_XA_USB_DBG_TOP_P
D3001
D3002
D3003
D3004
CRITICAL
DFN1006
PLACE_NEAR=U3000.19:10mm
PLACE_NEAR=U3000.18:10mm
PLACE_NEAR=U3000.15:10mm
PLACE_NEAR=U3000.16:10mm
RIDGE 0.9V SVR XW
XW3000
P0V9_TBT_X_SVR_AGND
NO_XNET_CONNECTION=1
R3082 0
PP1V8_AWAKE
30K
PPVBUS_USBC_XA
SOC_USB_VBUS
USB VBUS detection
<radar://25149752>
R3080 NOSTUFF
DZ3000 BZT52C3V0LP
DFN10062
TBT to ACE
TBT
Alpine Ridge U2800
(MASTER)
I2C_TBT_X_SCL
I2C_TBT_X_SDA
I2C_TBT_XA_INT_L
I2C_TBT_XB_INT_L
Pri ACE
U3100
(Write: 0x70 Read: 0x71)
Sec ACE
U3200
(Write: 0x7E Read: 0x7F)
Ridge PCIE Caps
PCIE_TBT_X_R2D_C_P<0>
PCIE_TBT_X_R2D_C_N<0>
PCIE_TBT_X_R2D_C_P<1>
PCIE_TBT_X_R2D_C_N<1>
PCIE_TBT_X_R2D_C_P<2>
PCIE_TBT_X_R2D_C_N<2>
PCIE_TBT_X_R2D_C_P<3>
PCIE_TBT_X_R2D_C_N<3>
PCIE_TBT_X_R2D_P<0>
PCIE_TBT_X_R2D_N<0>
PCIE_TBT_X_R2D_P<1>
PCIE_TBT_X_R2D_N<1>
PCIE_TBT_X_R2D_P<2>
PCIE_TBT_X_R2D_N<2>
PCIE_TBT_X_R2D_P<3>
PCIE_TBT_X_R2D_N<3>
PCIE_TBT_X_D2R_P<0>
PCIE_TBT_X_D2R_N<0>
PCIE_TBT_X_D2R_P<1>
PCIE_TBT_X_D2R_N<1>
PCIE_TBT_X_D2R_P<2>
PCIE_TBT_X_D2R_N<2>
PCIE_TBT_X_D2R_P<3>
PCIE_TBT_X_D2R_N<3>
GND_VOID=TRUE
C3040 0.22UF
C3041 0.22UF
C3042 0.22UF
C3043 0.22UF
C3044 0.22UF
C3045 0.22UF
C3046 0.22UF
C3047 0.22UF
C3050 0.22UF
C3051 0.22UF
C3052 0.22UF
C3053 0.22UF
C3054 0.22UF
C3055 0.22UF
C3056 0.22UF
C3057 0.22UF
Place all Caps close to Transmitters
R2D ones close to CPU, D2R ones to TBT.
BOM_COST_GROUP=USB-C
PAGE TITLE
USB-C (X) Support
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
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SHEET 28 OF 115
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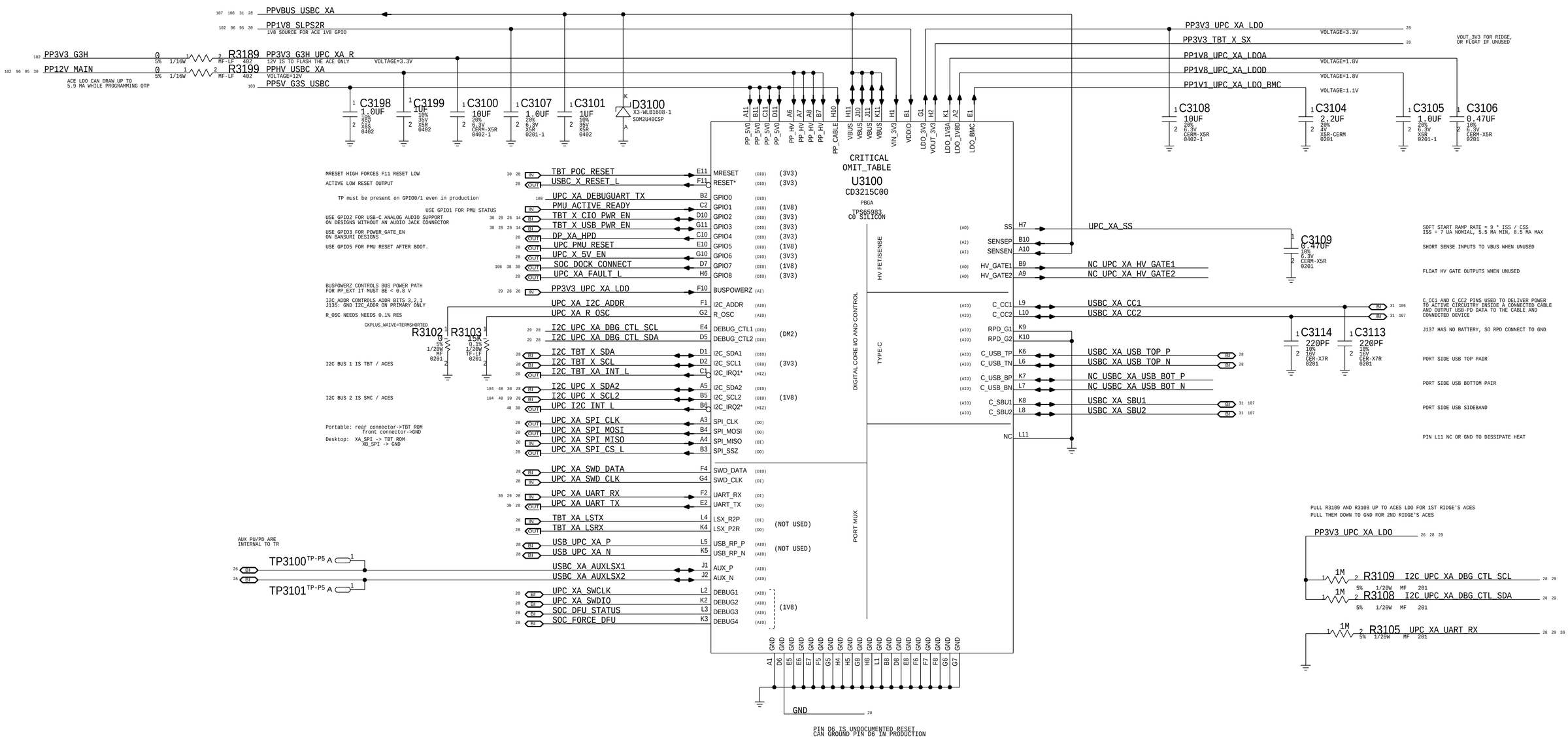
X PRIMARY ACE USB-C PORT CONTROLLER (UPC)

J137 USBC SUPPORTS 5V @ 3A
PP12V IS FOR PROGRAMMING ACE ONLY



NOTE:
DEBUG MUX IS CONNECTED TO PRIMARY ACE OF 1ST RIDGE (XA ACE)
R3752-R3755, R3790-R3792 ARE OPTIONAL

BOM_COST_GROUP=USB-C

NOT SYNCED TO OTHER PLATFORMS
Mary
SYNC_DATE=04/26/2018

PAGE TITLE	PAGE_TITLE=USB-C (X) PORT CONTROLLER A
Apple Inc.	DRAWING NUMBER 051-02424 SIZE D
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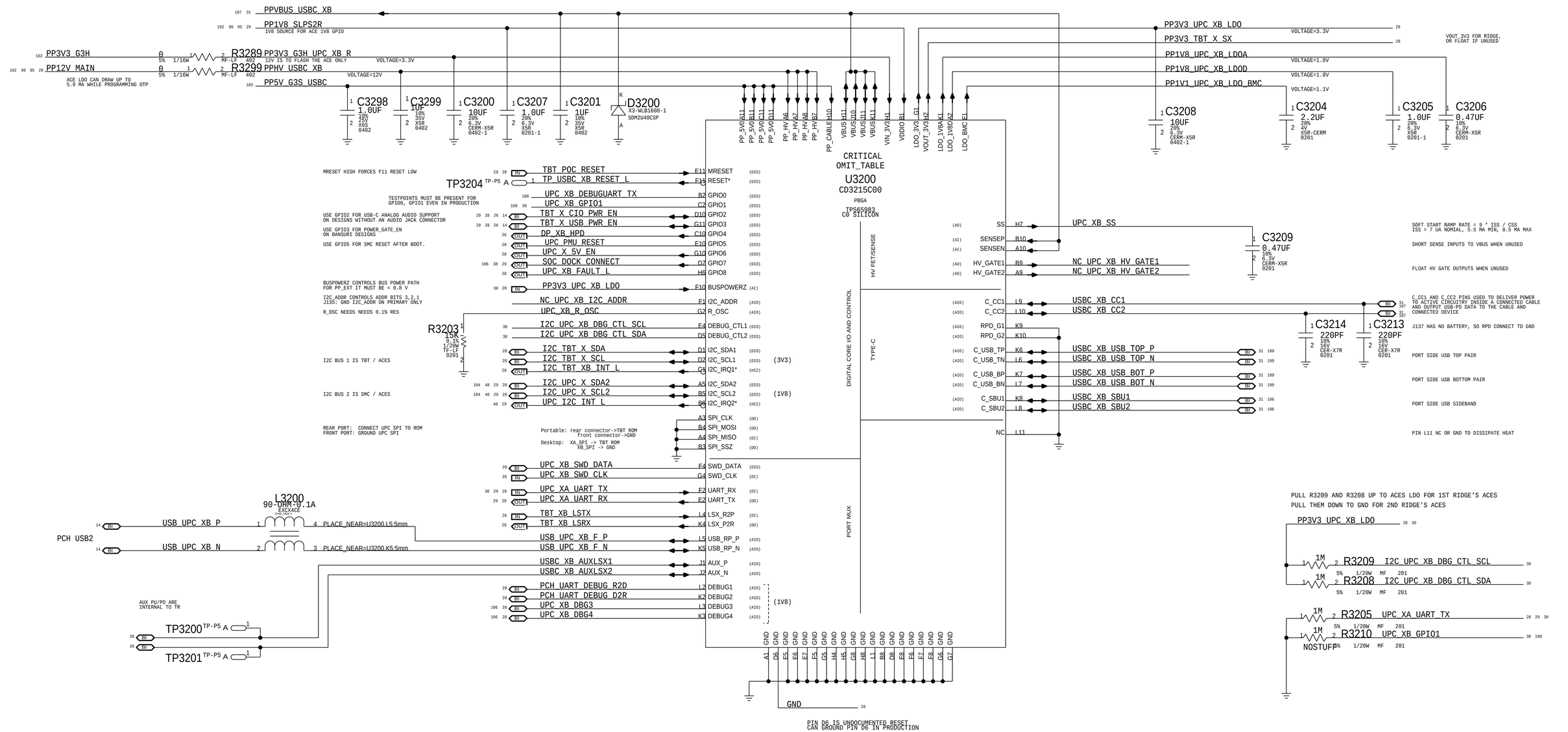
X SECONDARY ACE1 USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

NOT SYNCED TO OTHER PLATFORMS
Mary
SYNC_DATE=04/26/2018

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Apple Inc.	DRAWING NUMBER 051-02424 SIZE D
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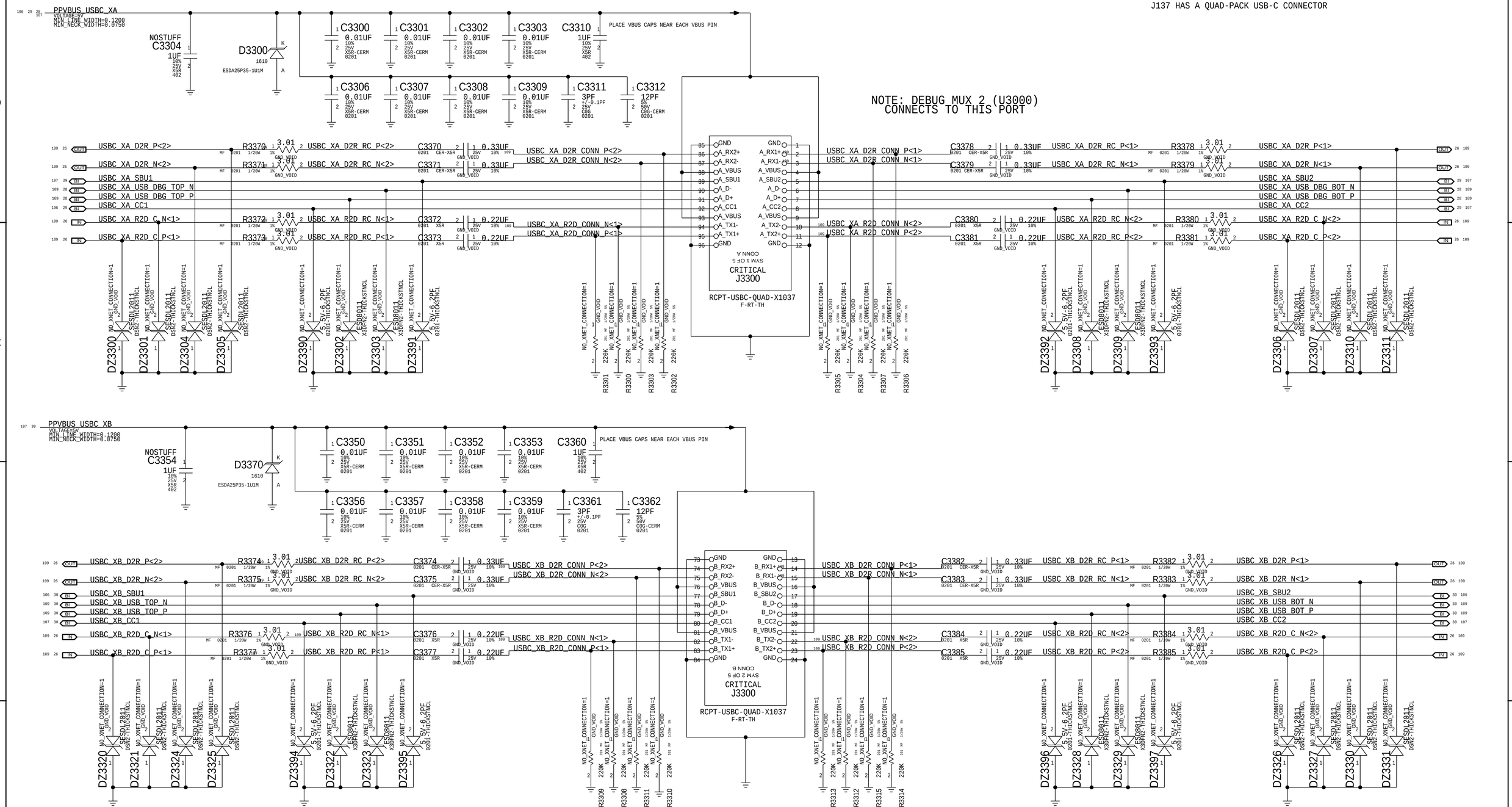
J137 SUPPORTS 5V @ 3A

J137 HAS A QUAD-PACK USB-C CONNECTOR

NOTE: DEBUG MUX 2 (U3000) CONNECTS TO THIS PORT



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SYNC_MASTER=Mary	SYNC_DATE=04/26/2018
PAGE TITLE	USB-C (X) CONNECTORS
Apple Inc.	DRAWING NUMBER 051-02424 SIZE D
	REVISION 6.0.0
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PLACE HOLDER

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

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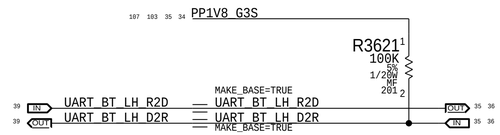
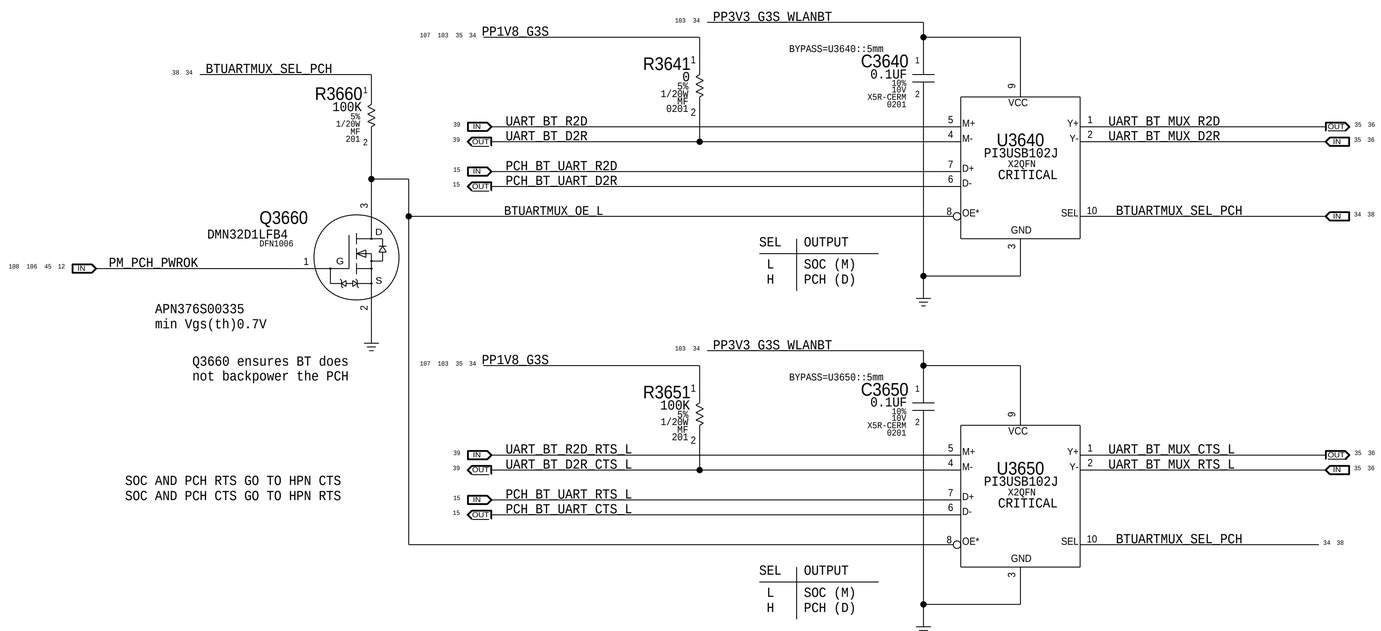
BOM_COST_GROUP=DEBUG

Software	I2S_SEL	UART_SEL	UART I/F
Gen1 (macOS)	0	1	UART (PCH)
Gen2	X	0	UART (SOC)

BT_DEV_WAKE option





SOC AND PCH RTS GO TO HPN CTS
SOC AND PCH CTS GO TO HPN RTS

BOM_COST_GROUP=WIRELESS

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
WIFI/BT: Support

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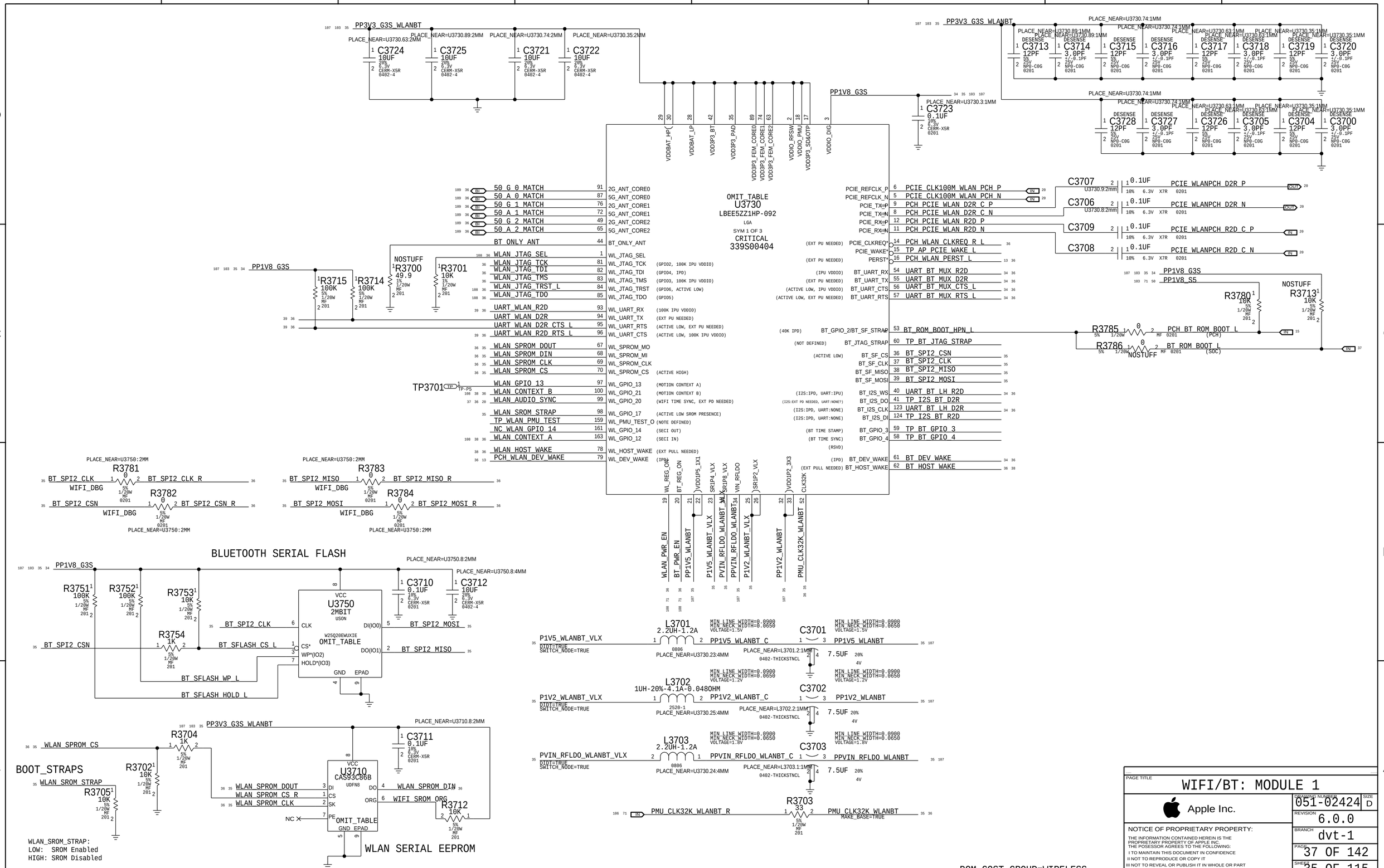
PP3V3_G3S_WLANBT
C3724 10UF 20% 6.3V CERM-X5R 0402-4
C3725 10UF 20% 6.3V CERM-X5R 0402-4
C3721 10UF 20% 6.3V CERM-X5R 0402-4
C3722 10UF 20% 6.3V CERM-X5R 0402-4
PP1V8_G3S
C3723 0.1UF 10% 6.3V CERM-X5R 0201
C3713 12PF 5% 25V NP0-C0G 0201
C3714 3.0PF +/-0.1PF 25V NP0-C0G 0201
C3715 12PF 5% 25V NP0-C0G 0201
C3716 3.0PF +/-0.1PF 25V NP0-C0G 0201
C3717 12PF 5% 25V NP0-C0G 0201
C3718 3.0PF +/-0.1PF 25V NP0-C0G 0201
C3719 12PF 5% 25V NP0-C0G 0201
C3720 3.0PF +/-0.1PF 25V NP0-C0G 0201
C3728 12PF 5% 25V NP0-C0G 0201
C3727 3.0PF +/-0.1PF 25V NP0-C0G 0201
C3726 12PF 5% 25V NP0-C0G 0201
C3705 3.0PF +/-0.1PF 25V NP0-C0G 0201
C3704 3.0PF +/-0.1PF 25V NP0-C0G 0201
C3700 3.0PF +/-0.1PF 25V NP0-C0G 0201
OMIT_TABLE
U3730
LBEE5ZZ1HP-092
LGA
SYM 1 OF 3
CRITICAL
339S00404
VDDBAT_HP
VDDBAT_LP
VDD3P3_BT
VDD3P3_PAD
VDD3P3_FEM_CORE0
VDD3P3_FEM_CORE1
VDD3P3_FEM_CORE2
VDDIO_RFSW
VDDIO_PMU
VDD3P3_SDKOTP
VDDIO_DIG
2G_ANT_CORE0
5G_ANT_CORE0
2G_ANT_CORE1
5G_ANT_CORE1
2G_ANT_CORE2
5G_ANT_CORE2
BT_ONLY_ANT
WL_JTAG_SEL
WL_JTAG_TCK (GPIO2, 100K IPU VDDIO)
WL_JTAG_TDI (GPIO4, IPD)
WL_JTAG_TMS (GPIO3, 100K IPU VDDIO)
WL_JTAG_TRST (GPIO6, ACTIVE LOW)
WL_JTAG_TDO (GPIO5)
WL_UART_RX (100K IPU VDDIO)
WL_UART_TX (EXT PU NEEDED)
WL_UART_RTS (ACTIVE LOW, EXT PU NEEDED)
WL_UART_CTS (ACTIVE LOW, 100K IPU VDDIO)
WL_SPROM_MO
WL_SPROM_MI
WL_SPROM_CLK
WL_SPROM_CS (ACTIVE HIGH)
WL_GPIO_13 (MOTION CONTEXT A)
WL_GPIO_21 (MOTION CONTEXT B)
WL_GPIO_20 (WIFI TIME SYNC, EXT PD NEEDED)
WL_GPIO_17 (ACTIVE LOW SROM PRESENCE)
WL_PMU_TEST_O (NOTE DEFINED)
WL_GPIO_14 (SECI OUT)
WL_GPIO_12 (SECI IN)
WL_HOST_WAKE (EXT PULL NEEDED)
WL_DEV_WAKE (IPD)
WL_REG_ON
BT_REG_ON
VDDIP5_1X1
SR1P4_VLX
SR1P8_VLX
VIN_RFLDO
SR1P2_VLX
VDDIP2_3X3
CLK32K
WLAN_PWR_EN
BT_PWR_EN
PP1V5_WLANBT
P1V5_WLANBT_VLX
PVIN_RFLDO_WLANBT_VLX
PPVIN_RFLDO_WLANBT
P1V2_WLANBT_VLX
PP1V2_WLANBT
PMU_CLK32K_WLANBT
PCIE_REFCLK_P
PCIE_REFCLK_N
PCIE_TX0P
PCIE_TX0N
PCIE_RX0P
PCIE_RX0N
PCIE_CLKREQ* (EXT PU NEEDED)
PCIE_WAKE* (EXT PU NEEDED)
PERST* (IPU VDDIO)
BT_UART_RX (EXT PU NEEDED)
BT_UART_TX (ACTIVE LOW, IPU VDDIO)
BT_UART_CTS (ACTIVE LOW, EXT PU NEEDED)
BT_UART_RTS
BT_GPIO_2/BT_SF_STRAP (40K IPD)
BT_JTAG_STRAP (NOT DEFINED)
BT_SF_CS (ACTIVE LOW)
BT_SF_CLK
BT_SF_MISO
BT_SF_MOSI
BT_I2S_WS (I2S:IPD, UART:IPU)
BT_I2S_DO (I2S:EXT PD NEEDED, UART:NONE?)
BT_I2S_CLK (I2S:IPD, UART:NONE)
BT_I2S_DI (I2S:IPD, UART:NONE)
BT_GPIO_3 (BT TIME STAMP)
BT_GPIO_4 (BT TIME SYNC)
(RSVD)
BT_DEV_WAKE (IPD)
BT_HOST_WAKE (EXT PULL NEEDED)
PCIE_CLK100M_WLAN_PCH_P
PCIE_CLK100M_WLAN_PCH_N
PCH_PCIE_WLAN_D2R_C_P
PCH_PCIE_WLAN_D2R_C_N
PCH_PCIE_WLAN_R2D_P
PCH_PCIE_WLAN_R2D_N
PCH_WLAN_CLKREQ_R_L
TP_AP_PCIE_WAKE_L
PCH_WLAN_PERST_L
UART_BT_MUX_R2D
UART_BT_MUX_D2R
UART_BT_MUX_CTS_L
UART_BT_MUX_RTS_L
BT_ROM_BOOT_HPN_L
TP_BT_JTAG_STRAP
BT_SPI2_CSN
BT_SPI2_CLK
BT_SPI2_MISO
BT_SPI2_MOSI
UART_BT_LH_R2D
TP_I2S_BT_D2R
UART_BT_LH_D2R
TP_I2S_BT_R2D
TP_BT_GPIO_3
TP_BT_GPIO_4
BT_DEV_WAKE
BT_HOST_WAKE
50_G_0_MATCH
50_A_0_MATCH
50_G_1_MATCH
50_A_1_MATCH
50_G_2_MATCH
50_A_2_MATCH
WLAN_JTAG_SEL
WLAN_JTAG_TCK
WLAN_JTAG_TDI
WLAN_JTAG_TMS
WLAN_JTAG_TRST_L
WLAN_JTAG_TDO
UART_WLAN_R2D
UART_WLAN_D2R
UART_WLAN_D2R_CTS_L
UART_WLAN_R2D_RTS_L
WLAN_SPROM_DOUT
WLAN_SPROM_DIN
WLAN_SPROM_CLK
WLAN_SPROM_CS
WLAN_GPIO_13
WLAN_CONTEXT_B
WLAN_AUDIO_SYNC
WLAN_SROM_STRAP
TP_WLAN_PMU_TEST
NC_WLAN_GPIO_14
WLAN_CONTEXT_A
WLAN_HOST_WAKE
PCH_WLAN_DEV_WAKE
TP3701
NOSTUFF
R3700 49.9 1% 1/20W MF 201
R3701 10K 1% 1/20W MF 201
R3715 100K 5% 1/20W MF 201
R3714 100K 5% 1/20W MF 201
C3707 0.1UF 10% 6.3V X7R 0201
C3706 0.1UF 10% 6.3V X7R 0201
C3709 0.1UF 10% 6.3V X7R 0201
C3708 0.1UF 10% 6.3V X7R 0201
PCIE_WLANPCH_D2R_P
PCIE_WLANPCH_D2R_N
PCIE_WLANPCH_R2D_C_P
PCIE_WLANPCH_R2D_C_N
PP1V8_S5
R3780 10K 5% 1/20W MF 201
R3713 10K 5% 1/20W MF 201
R3785 0 5% 1/20W MF 0201 (PCH)
R3786 0 5% 1/20W MF 0201 (SOC)
PCH_BT_ROM_BOOT_L
BT_ROM_BOOT_L
PLACE_NEAR=U3750:2MM
R3781 0 5% 1/20W MF 0201
R3782 0 5% 1/20W MF 0201
R3783 0 5% 1/20W MF 0201
R3784 0 5% 1/20W MF 0201
WIFI_DBG
BT_SPI2_CLK_R
BT_SPI2_CSN_R
BT_SPI2_MISO_R
BT_SPI2_MOSI_R
BLUETOOTH SERIAL FLASH
PLACE_NEAR=U3750.8:2MM
PLACE_NEAR=U3750.8:4MM
R3751 100K 5% 1/20W MF 201
R3752 100K 5% 1/20W MF 201
R3753 10K 5% 1/20W MF 201
R3754 1K 5% 1/20W MF 201
C3710 0.1UF 10% 6.3V CERM-X5R 0201
C3712 10UF 20% 6.3V CERM-X5R 0402-4
U3750
2MBIT
USON
W25Q20EWUXIE
OMIT_TABLE
VCC
CLK
CS*
WP*(IO2)
HOLD*(IO3)
DI(IO0)
DO(IO1)
GND
EPAD
BT_SFLASH_CS_L
BT_SFLASH_WP_L
BT_SFLASH_HOLD_L
PP3V3_G3S_WLANBT
PLACE_NEAR=U3710.8:2MM
R3704 1K 5% 1/20W MF 201
R3702 10K 5% 1/20W MF 201
R3705 10K 5% 1/20W MF 201
BOOT_STRAPS
WLAN_SROM_STRAP
WLAN_SPROM_CS
WLAN_SPROM_DOUT
WLAN_SPROM_CS_R
WLAN_SPROM_CLK
C3711 0.1UF 10% 6.3V CERM-X5R 0201
U3710
CAS93C86B
UDFN8
DI
CS
SK
PE
DO
ORG
NC
WLAN_SPROM_DIN
WIFI_SROM_ORG
R3712 10K 5% 1/20W MF 201
WLAN_SROM_STRAP:
LOW: SROM Enabled
HIGH: SROM Disabled
WLAN SERIAL EEPROM
L3701 2.2UH-1.2A 0806
L3702 1UH-20%-4.1A-0.048OHM 2520-1
L3703 2.2UH-1.2A 0806
C3701 7.5UF 20% 4V 0402-THICKSTNCL
C3702 7.5UF 20% 4V 0402-THICKSTNCL
C3703 7.5UF 20% 4V 0402-THICKSTNCL
P1V5_WLANBT_VLX
PP1V5_WLANBT_C
PP1V5_WLANBT
P1V2_WLANBT_VLX
PP1V2_WLANBT_C
PP1V2_WLANBT
PVIN_RFLDO_WLANBT_VLX
PPVIN_RFLDO_WLANBT_C
PPVIN_RFLDO_WLANBT
R3703 33 5% 1/20W MF 201
PMU_CLK32K_WLANBT_R
PMU_CLK32K_WLANBT
BOM_COST_GROUP=WIRELESS
PAGE TITLE
WIFI/BT: MODULE 1
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 37 OF 142
SHEET 35 OF 115
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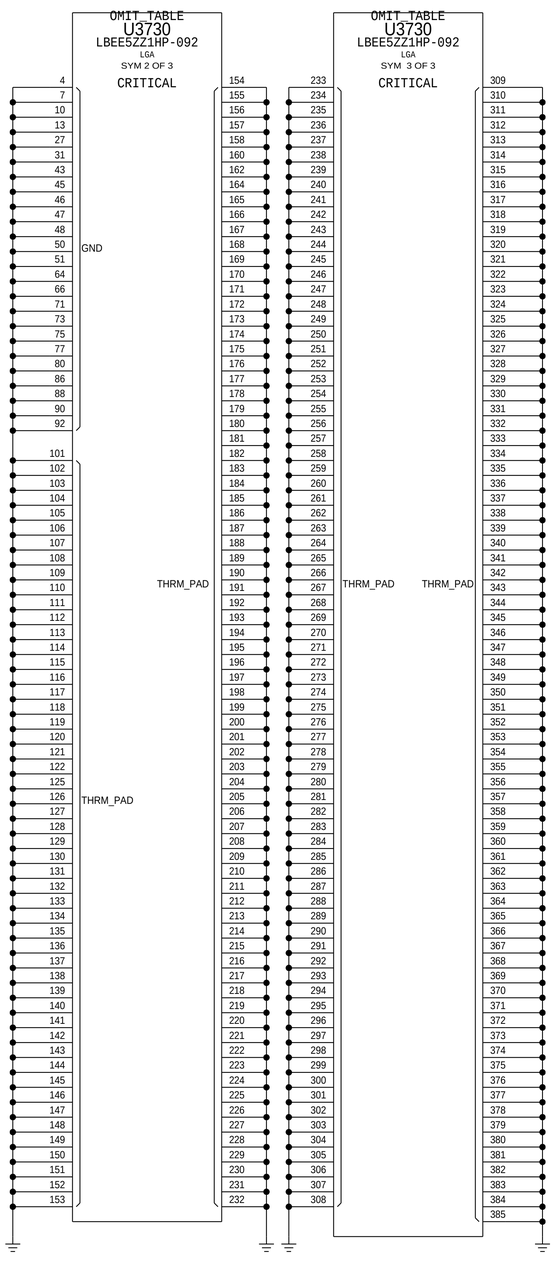
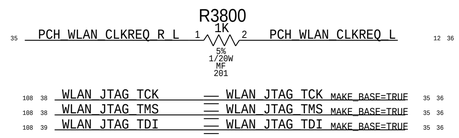
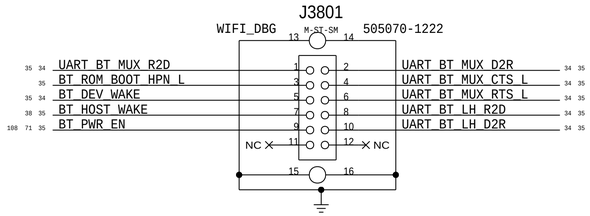
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00152	1	IND,0.9NH,1,1A,0201	L3810	CRITICAL	
131S0631	1	CAP,CER,0.3pF,0201	C3817,C3827	CRITICAL	
152S00153	1	IND,1NH,1,1A,0201	L3820	CRITICAL	
152S1222	1	IND,3NH,1,1A,0201	C3812	CRITICAL	
131S0555	1	cap,CER,1pF,0201	L3811	CRITICAL	

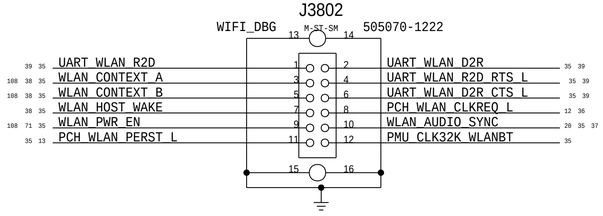


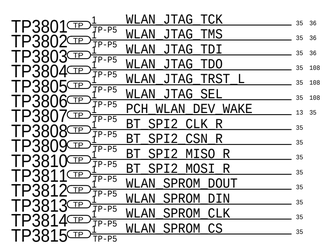


BT ARKANOID CONN



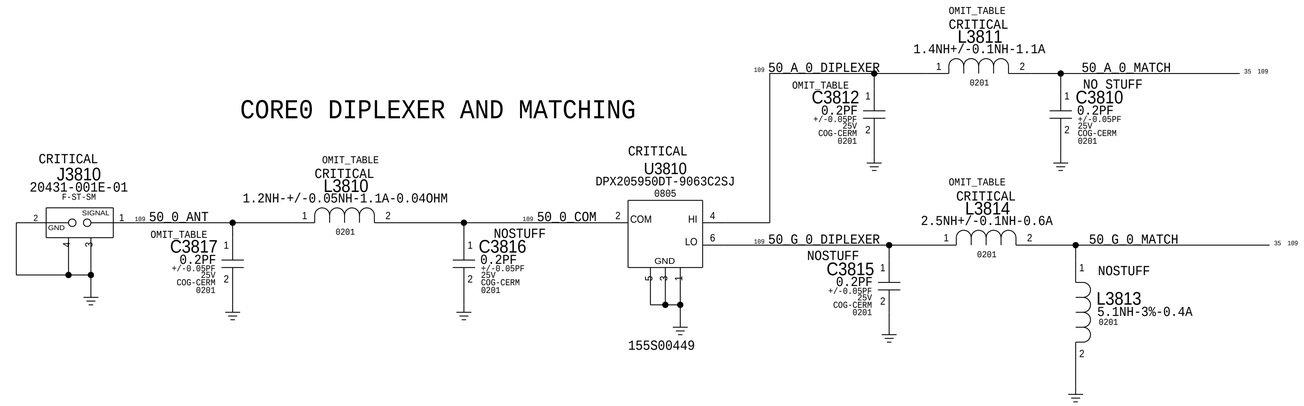
WLAN ARKANOID CONN



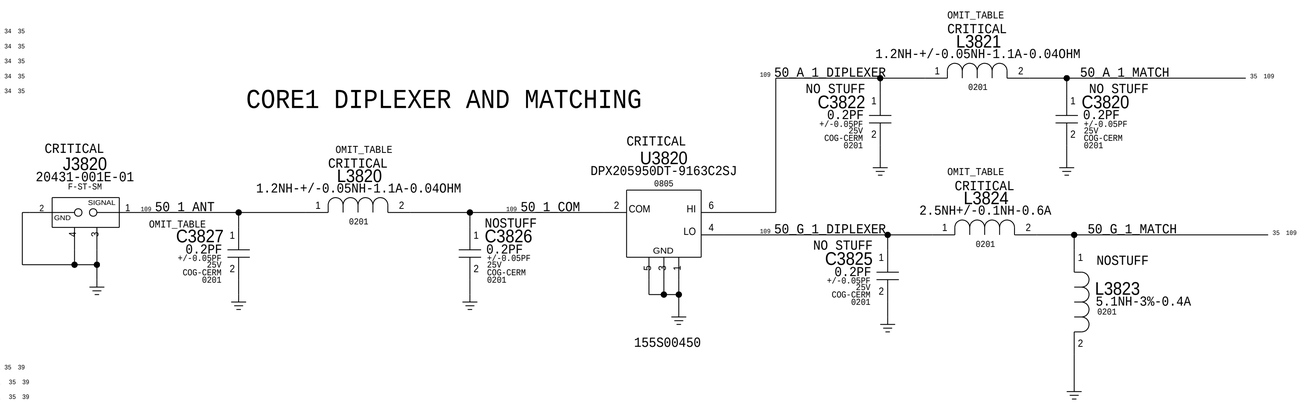


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	5	RES,MF,0 OHM,0.5%,0201	L3814,L3821,L3824,L3831,L3834	CRITICAL	

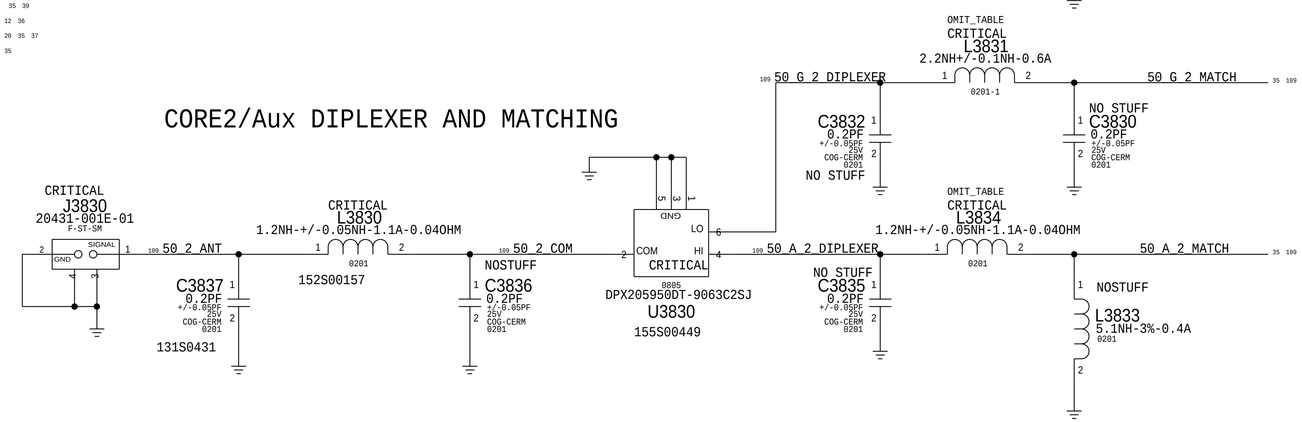
CORE0 DIPLEXER AND MATCHING



CORE1 DIPLEXER AND MATCHING



CORE2/Aux DIPLEXER AND MATCHING



BOM_COST_GROUP=WIRELESS

PAGE TITLE
WIFI/BT: MODULE 2

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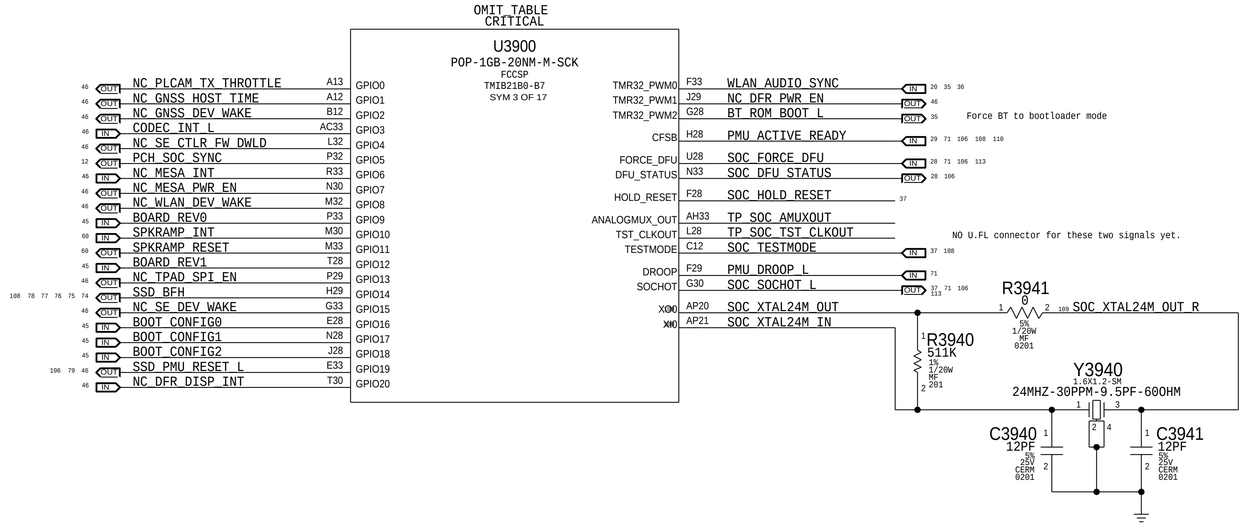
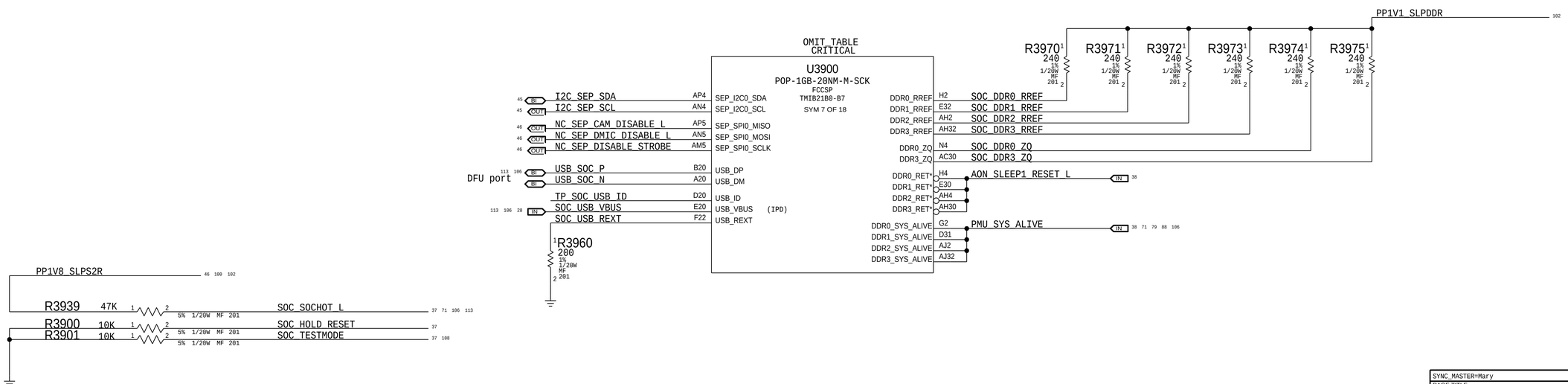
Note 1) IPU represents SW configured state, not HW default





BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
SoC GPIO/SEP/USB/DDR/Test

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
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OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
SYM 6 OF 17

108 36 35	OUT	WLAN_CONTEXT_A	B5	AOP_FUNC[0]			
108 36 35	OUT	WLAN_CONTEXT_B	D4	AOP_FUNC[1]			
46	IN	NC_GYRO_INT1	G1	AOP_FUNC[2]	(IPD)	(IPU)	
46	IN	NC_GYRO_INT2	C5	AOP_FUNC[3]	(IPD)	(IPU)	
34	OUT	BTUARTMUX_SEL_PCH	D1	AOP_FUNC[4]			
15	IN	SOC_PERST_L	E4	AOP_FUNC[5]			
46	IN	NC_ALTIMETER_INT	C4	AOP_FUNC[6]	(IPD)		
46	OUT	NC_SPI_GYRO_CS_L	F4	AOP_FUNC[7]			
46	OUT	NC_SPI_ALTIMETER_CS_L	E1	AOP_FUNC[8]			
48	OUT	NC_I2C_AOP_SCL	H6	AOP_I2C0_SCL			
48	BI	NC_I2C_AOP_SDA	G6	AOP_I2C0_SDA			

AOP_PDM_CLK0	N6	NC_PDM_DMIC_CLK0_R	OUT	46			
AOP_PDM_CLK1	J6	NC_PDM_DMIC_CLK1_R	OUT	46			
AOP_PDM_CLK2	F5	SMC_FIXTURE_MODE_L	IN	TP is needed on Dev_Supply			
AOP_PDM_CLK3	F2	NC_PLCAM_PROX_INT_L	IN	46			
AOP_PDM_CLK4	J4	NC_PLCAM_ROMEO_B2B_DETECT	IN	46			
AOP_PDM_DATA0	F1	NC_PDM_DMIC_DATA0	IN	46			
AOP_PDM_DATA1	J1	NC_PDM_DMIC_DATA1	IN	46			
AOP_SPI_MOSI	A5	NC_SPI_AOP_SENSOR_MOSI_R	OUT	46			
AOP_SPI_SCLK	E5	NC_SPI_AOP_SENSOR_CLK_R	OUT	46			
AOP_SPI_MISO	C2	NC_SPI_AOP_SENSOR_MISO	IN	46			

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
SYM 5 OF 17

46	IN	NC_DFR_TOUCH_INT_L	AG6	AON_GPIO0			
20	IN	CPU_SMC_THRMTRIP_L	AB6	AON_GPIO1			
46	IN	NC_SMC_GFX_SELF_THROTTLE	AL1	AON_GPIO2	(IPD)		
46	OUT	NC_SMC_TOPBLK_SWP_L	AH5	AON_GPIO3			
18	IN	XDP_PRESENT_L	AG1	AON_GPIO4			
46	OUT	CODEC_RESET_L	AL4	AON_GPIO5			
34	OUT	SOC_BT_DEV_WAKE	AK4	AON_GPIO6			
84	IN	PCIEDN_WAKE_L	AD6	AON_GPIO7	(IPU)		
81 20	OUT	ENET_LOW_PWR	AM1	AON_GPIO8			
100	IN	TPAD_SPI_INT_L_ACDC_ID	AJ6	AON_GPIO9			
46	IN	NC_SDCONN_STATE_CHANGE_L	AK5	AON_GPIO10	(IPU)		
84	IN	ENET_MEDIA_SENSE	AJ1	AON_GPIO11	(IPD)		
71	IN	PMU_INT_L	AL6	AON_GPIO12	(IPU)		
		SPMI_CLK_R	AA6	AON_SPMI_SCLK			
		SPMI_DATA_R	AK2	AON_SPMI_SDATA			
106 71	IN	PMU_CLK32K_SOC	AK6	RT_CLK32768			
		SOC_COLD_RESET_L	AG4	COLD_RESET*			
			AF4	CFSB_AON			
108 106 71	IN	PMU_COLD_RESET_L					

				JTAG_TCK	(IPU)	AF6	SWD_SOC_SWCLK
				JTAG_TMS	(IPU)	AH1	SWD_SOC_SWDIO
				JTAG_TDI	(IPU)	AE6	DEBUG_JTAG_SOC_TDI
				JTAG_TDO		AK1	DEBUG_JTAG_SOC_TDO
				JTAG_TRST*	(IPD)	AH6	TP_JTAG_SOC_TRST_L
				JTAG_SEL		Y8	SOC_JTAG_SEL (DAP=0, TAP=1)
				DOCK_CONNECT		AJ5	SOC_DOCK_CONNECT
				AON_SWD0_TMS		AF2	WLAN_JTAG_TMS
				AON_SWD1_TMS	(IPU)	AE4	NC_MESA_MENUKEY_L
				AON_SWD01_TCK		AE5	WLAN_JTAG_TCK
				WDOG		AF5	SOC_WDOG
				AON_SLEEP1_RESET*		AC6	AON_SLEEP1_RESET_L

IN	46 108 113	SWD_SOC_SWCLK	AH1	SWD_SOC_SWDIO	BI
BI	46 108 113	DEBUG_JTAG_SOC_TDI	AE6	DEBUG_JTAG_SOC_TDO	106 113
106 113		TP_JTAG_SOC_TRST_L	AH6	JTAG_TRST*	108
108		SOC_JTAG_SEL	Y8	JTAG_SEL	38 108
IN	29 30 38 106	SOC_DOCK_CONNECT	AJ5	DOCK_CONNECT	
BI	36 108	WLAN_JTAG_TMS	AF2	AON_SWD0_TMS	
IN	46	NC_MESA_MENUKEY_L	AE4	AON_SWD1_TMS	
OUT	36 108	WLAN_JTAG_TCK	AE5	AON_SWD01_TCK	
OUT	71 106	SOC_WDOG	AF5	WDOG	
OUT	37	AON_SLEEP1_RESET_L	AC6	AON_SLEEP1_RESET*	

PLACE_NEAR=U3900.AA6:5MM
PLACE_NEAR=U7800.W7:5MM

71	OUT	SPMI_CLK	R4036	20	5%	1/20W	MF	201
71	BI	SPMI_DATA	R4037	20	5%	1/20W	MF	201

R4039 4.7K 5% 1/20W MF 201

OMIT_TABLE
CRITICAL

U3900
POP-1GB-20NM-M-SCK
FCCSP
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PLACE_NEAR=U3900.R4:5MM
PLACE_NEAR=U3900.R1:5MM
PLACE_NEAR=U3900.T5:5MM
PLACE_NEAR=U3900.T6:5MM

113 109 38 12	BI	ESPI_IO<0>	R4050	20	5%	1/20W	MF	201	109 ESPI_IO_R<0>
113 109 38 12	BI	ESPI_IO<1>	R4051	20	5%	1/20W	MF	201	109 ESPI_IO_R<1>
113 109 38 12	BI	ESPI_IO<2>	R4052	20	5%	1/20W	MF	201	109 ESPI_IO_R<2>
113 109 38 12	BI	ESPI_IO<3>	R4053	20	5%	1/20W	MF	201	109 ESPI_IO_R<3>

113 109 12	IN	ESPI_CLK	P2	SMC_ESPI_CLK	(IPD)
113 38 12	IN	ESPI_CS_L	T4	SMC_ESPI_CS*	
113 12	IN	ESPI_RESET_L	T2	SMC_ESPI_RESET*	(IPD)
46 45	IN	SMC_PECI_RX	M6	SMC_PECI_IN	(IPD)
45	OUT	SMC_PECI_TX	R6	SMC_PECI_OUT	
108 45	OUT	SMC_PCH_PWROK	U7	PCH_PWROK	
108 45	OUT	SMC_PCH_SYS_PWROK	U8	SYS_PWROK	
45	OUT	SMC_RSMRST_L	U1	RSMRST*	
108 106 45	OUT	SMC_SYSRST_L	U5	SYS_RESET*	
106 100 71 12	IN	PM_SLP_S0_L	W1	SLP_S0B	
63 46 45	BI	SMC_PROCHOT_L	P6	PROCHOT*	
106 88 79 71 37	IN	PMU_SYS_ALIVE	W6	SYS_ALIVE	
106 48	OUT	I2C_UPC_SCL	K4	SMC_I2C0_SCL	
106 48	BI	I2C_UPC_SDA	H1	SMC_I2C0_SDA	
48	OUT	NC_I2C_SNS0_S0_SCL	L4	SMC_I2C1_SCL	
48	BI	NC_I2C_SNS0_S0_SDA	L5	SMC_I2C1_SDA	
48	OUT	I2C_SNS1_S0_SCL	M4	SMC_I2C2_SCL	
48	BI	I2C_SNS1_S0_SDA	K1	SMC_I2C2_SDA	
48	OUT	I2C_DISP_SCL	L2	SMC_I2C3_SCL	
48	BI	I2C_DISP_SDA	P5	SMC_I2C3_SDA	
106 48	OUT	I2C_PWR_SCL	L1	SMC_I2C4_SCL	
106 48	BI	I2C_PWR_SDA	M1	SMC_I2C4_SDA	
48	OUT	NC_I2C_IOSNS_SCL	N1	SMC_I2C5_SCL	
48	BI	NC_I2C_IOSNS_SDA	N2	SMC_I2C5_SDA	
108 48	OUT	I2C_SSD_SCL	P1	SMC_I2C6_SCL	(IPU)
108 48	BI	I2C_SSD_SDA	P4	SMC_I2C6_SDA	

SMC_GPIO0	V4	CODEC_WAKE_L	IN	46	
SMC_GPIO1	V8	BT_HOST_WAKE	IN	35 36	
SMC_GPIO2	V6	WLAN_HOST_WAKE	IN	35 36	(IPD)
SMC_GPIO3	U4	SMC_GFX_THROTTLE_L	OUT	46	
SMC_GPIO4	V7	LIDINT_L_UARTHDD_D2R	IN	46	
SMC_GPIO5	U6	PCC_EVENT	BI	108	
SMC_GPIO6	V1	DP2HDMI_AOP_VDD12ON	IN	46	
SMC_GPIO7	W5	PSU11VOC_WAKE_L	IN	46	
SMC_GPIO8	AC1	LIDOPEN_PSU12VPGOOD_ACDCBURST_L	BI	100 108	
SMC_GPIO9	AB2	NC_SPI_DESCRIPTOR_OVERRIDE_L	OUT	46	
SMC_GPIO10	AB1	NC_DISP_GCON_INT_L	IN	46	(IPU)
SMC_GPIO11	AA4	PCH_GCON_INT_L		15	
SMC_GPIO12	W8	PSU_P12V_EN_L	OUT	46	
SMC_GPIO13	AA1	TBT_WAKE_L	IN	28	(IPU)
SMC_GPIO14	AC2	UPC_I2C_INT_L	IN	28 48 94	(IPU)
SMC_GPIO_15	K2	TP_SMC_DEBUG	IN	46	
SMC_ADC0	AE1	SMC_P12VIN_VSENSE	IN	46	
SMC_ADC1	Y5	SMC_P12VIN_ISENSE	IN	46	
SMC_ADC2	AE2	SMC_CPU_HI_ISENSE	IN	46	
SMC_ADC3	AB5	SMC_CPU_VCC_ISENSE	IN	46	
SMC_ADC4	Y7	SMC_CPU_VCC_VSENSE	IN	46	
SMC_ADC5	AD4	SMC_CPUGT_VSENSE	IN	46	
SMC_ADC6	AF1	SMC_CPUGT_ISENSE	IN	46	
SMC_ADC7	Y6	SMC_P1V2_ISENSE	IN	46	
REFP_ADC	AC5	PP1V25_SLPS2R_SMC_AVREF		45	
REFM_ADC	AC4	GND_SMC_AVSS			
SMC_PWM0	E2	SMC_FAN_0_PWM	OUT	57	
SMC_TACH0	K6	SMC_FAN_0_TACH	IN	57	
SMC_PWM1	N5	NC_SMC_FAN_1_PWM	OUT	46	
SMC_TACH1	L6	NC_SMC_FAN_1_TACH	IN	46	
SMC_PWM2	K5	SMC_LED_ONEWIRE	BI	46	
SMC_UART0_RXD	U2	SMC_DEBUGPRT_RX	IN	95 113	(IPU)
SMC_UART0_TXD	T1	SMC_DEBUGPRT_TX	OUT	95 113	
SWD_OUT0_TCK	AB4	SSD0_SWCLK_UART_R2D	OUT	74 75 76 77 78 108	
SWD_OUT0_TMS	Y1	SSD0_SWDIO_UART_D2R	BI	74 75 76 77 78 108	
SWD_OUT1_TCK	AD1	NC_SSD1_SWCLK_UART_R2D	OUT	46	
SWD_OUT1_TMS	W7	NC_SSD1_SWDIO_UART_D2R	BI	46	

XW4089
SM
PLACE_NEAR=U3900.AC4:4MM

PP1V8_S5 12 16 17 103

R4046	10K	5%	1/20W	MF	201	SOC_JTAG_SEL	38 108
R4047	100K	5%	1/20W	MF	201	SOC_DOCK_CONNECT	29 30 38 106
R4054	100K	5%	1/20W	MF	201	ESPI_IO<0>	12 38 109 113
R4055	100K	5%	1/20W	MF	201	ESPI_IO<1>	12 38 109 113
R4056	100K	5%	1/20W	MF	201	ESPI_IO<2>	12 38 109 113
R4057	100K	5%	1/20W	MF	201	ESPI_IO<3>	12 38 109 113
R4059	100K	5%	1/20W	MF	201	ESPI_CS_L	12 38 113

BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

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SoC AOP/AON/SMC

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U3900
POP-1GB-20NM-M-SCK
FCCSP
TMIB21B0-B7
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46 IN	GND	B24	MIPI0C_DATA0_P		
46 IN	GND	A24	MIPI0C_DATA0_N		
46 IN	GND	B22	MIPI0C_DATA1_P		
46 IN	GND	A22	MIPI0C_DATA1_N		
46 IN	GND	B23	MIPI0C_CLK_P		
46 IN	GND	A23	MIPI0C_CLK_N		
46 IN	GND	B25	MIPI1C_DATA0_P		
46 IN	GND	A25	MIPI1C_DATA0_N		
46 IN	GND	B27	MIPI1C_DATA1_P		
46 IN	GND	A27	MIPI1C_DATA1_N		
46 IN	GND	B26	MIPI1C_CLK_P		
46 IN	GND	A26	MIPI1C_CLK_N		
46 OUT	GND	B30	MIPID_DATA0_P		
46 OUT	GND	A30	MIPID_DATA0_N		
46 OUT	GND	B29	MIPID_CLK_P		
46 OUT	GND	A29	MIPID_CLK_N		
	SOC_MIPI0C_REXT	F23	MIPI0C_REXT		
	SOC_MIPI1C_REXT	F25	MIPI1C_REXT		
	SOC_MIPID_REXT	F26	MIPID_REXT		
		AC28	ISP_I2C0_SDA		NC_I2C_FTCAM_SDA BI 49
		AD33	ISP_I2C0_SCL		NC_I2C_FTCAM_SCL OUT 49
		AA29	ISP_I2C1_SDA		NC_I2C_PLCAM_SDA BI 49
		AD30	ISP_I2C1_SCL		NC_I2C_PLCAM_SCL OUT 49
		AF32	SENSOR0_CLK		NC_FTCAM_CLK12M_R OUT 46
		AF30	SENSOR0_RST		NC_FTCAM_RESET_L OUT 46
		AC29	SENSOR0_ISTRB		NC_DFR_TOUCH_RESET_L OUT 46
		AA28	SENSOR1_CLK		NC_PLCAM_RX_CLK12M_R OUT 46
		AB30	SENSOR1_RST		NC_PLCAM_RX_RESET_L OUT 46
		AA30	SENSOR1_ISTRB		NC_DFR_DISP_RESET_L OUT 46
		AB28	SENSOR2_CLK		NC_PLCAM_TX_CLK12M_R OUT 46
		AD28	SENSOR2_RST		NC_PLCAM_TX_RESET_L OUT 46
		W28	SENSOR_INT	(IPD)	NC_PLCAM_TX_INT IN 46
		D33	DISP_TE	(IPD)	NC_DFR_DISP_TE IN 46
		L30	DISP_VSYNC		BOARD_REV2 IN 45
		AF29	CLK32K_OUT		NC_DFR_TOUCH_CLK32K_RESET_L OUT 46

R4100 4.02K 1% 1/20W MF 201
R4101 4.02K 1% 1/20W MF 201
R4102 4.02K 1% 1/20W MF 201

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CRITICAL

U3900
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49 BI	I2C_SPKRAMP_SDA	W33	I2C0_SDA		
49 OUT	I2C_SPKRAMP_SCL	U30	I2C0_SCL		
49 BI	NC_I2C_SPKRAMP_R_SDA	AB32	I2C1_SDA		
49 OUT	NC_I2C_SPKRAMP_R_SCL	V30	I2C1_SCL		
49 BI	I2C_CODEC_SDA	H30	I2C2_SDA		
49 OUT	I2C_CODEC_SCL	P28	I2C2_SCL		
49 BI	NC_I2C_ALS_SDA	V28	I2C3_SDA		
49 OUT	NC_I2C_ALS_SCL	AB33	I2C3_SCL		
49 BI	NC_I2C_DFR_SDA	L33	I2C4_SDA		
49 OUT	NC_I2C_DFR_SCL	R29	I2C4_SCL		
49 BI	NC_I2C_SOC_5_SDA	M29	I2C5_SDA		
49 OUT	NC_I2C_SOC_5_SCL	R30	I2C5_SCL		
46 IN	NC_SPKR_ID1	J33	I2C6_SDA	(IPU)	
46 IN	NC_SPKR_ID0	L29	I2C6_SCL	(IPU)	
113 IN	SOC_DEBUGPRT_RX	V32	UART0_RXD	(IPU)	
113 OUT	SOC_DEBUGPRT_TX	U32	UART0_TXD		
46 IN	NC_UART_SE_D2R	B15	UART1_RXD		
46 OUT	NC_UART_SE_R2D	A15	UART1_TXD		
46 IN	NC_UART_SE_D2R_CTS_L	D13	UART1_CTS*		
46 OUT	NC_UART_SE_R2D_RTS_L	E12	UART1_RTS*		
34 IN	UART_BT_D2R	F32	UART2_RXD		
34 OUT	UART_BT_R2D	F30	UART2_TXD		
34 IN	UART_BT_D2R_CTS_L	M28	UART2_CTS*		
34 OUT	UART_BT_R2D_RTS_L	K28	UART2_RTS*		
34 IN	UART_BT_LH_D2R	H32	UART3_RXD		
34 OUT	UART_BT_LH_R2D	J32	UART3_TXD		
46 IN	NC_UART_GNSS_D2R_CTS_L	H33	UART3_CTS*		
46 OUT	NC_UART_GNSS_R2D_RTS_L	P30	UART3_RTS*		
36 35 IN	UART_WLAN_D2R	B14	UART4_RXD		
36 35 OUT	UART_WLAN_R2D	A14	UART4_TXD		
36 35 IN	UART_WLAN_D2R_CTS_L	C13	UART4_CTS*		
36 35 OUT	UART_WLAN_R2D_RTS_L	D12	UART4_RTS*		
		AN6	SPI0_MISO		SPI_SOCROM_MISO IN 45
		AM4	SPI0_MOSI		SPI_SOCROM_MOSI_R OUT 45
		AN3	SPI0_SCLK		SPI_SOCROM_CLK_R OUT 45
		AP6	SPI0_SSIN		SPI_SOCROM_CS_L_R OUT 45
		K30	SPI1_MISO	(IPU)	SPI_TPAD_MISO IN 45
		J30	SPI1_MOSI		SPI_TPAD_MOSI OUT 46
		K33	SPI1_SCLK		SPI_TPAD_CLK OUT 46
		R28	SPI1_SSIN		NC_SPI_TPAD_CS_L OUT 46
		B17	SPI2_MISO		NC_SPI_MESA_MISO IN 46
		C17	SPI2_MOSI		NC_SPI_MESA_MOSI_R OUT 46
		D16	SPI2_SCLK		NC_SPI_MESA_CLK_R OUT 46
		A17	SPI2_SSIN		WLAN_JTAG_TDI OUT 36 108
		C14	SPI3_MISO		NC_SPI_DFR_MISO IN 46
		D15	SPI3_MOSI		NC_SPI_DFR_MOSI_R OUT 46
		C16	SPI3_SCLK		NC_SPI_DFR_CLK_R OUT 46
		A16	SPI3_SSIN		NC_SPI_DFR_CS_L OUT 46
		Y28	I2S0_DIN	(IPD)	I2S_SPKRAMP_D2R_RR IN 46
		AC32	I2S0_DOUT		I2S_SPKRAMP_R2D_R OUT 46
		Y29	I2S0_BCLK		I2S_SPKRAMP_BCLK_R OUT 46
		AE32	I2S0_LRCK		I2S_SPKRAMP_LRCLK_R OUT 46
		AM33	I2S0_MCK		NC_DFR_TOUCH_RSVD BI 46
		C18	I2S1_DIN	(IPD)	I2S_SPKRAMP_R_D2R IN 46
		E17	I2S1_DOUT		I2S_SPKRAMP_R_R2D_R OUT 46
		D17	I2S1_BCLK		I2S_SPKRAMP_R_BCLK_R OUT 46
		B18	I2S1_LRCK		I2S_SPKRAMP_R_LRCLK OUT 46
		D18	I2S1_MCK		NC_PCHROM_SW_EN OUT 46
		Y33	I2S2_DIN	(IPD)	I2S_CODEC_D2R_RR IN 46
		AA33	I2S2_DOUT		I2S_CODEC_R2D_R OUT 46
		AE33	I2S2_BCLK		I2S_CODEC_BCLK_R OUT 46
		V29	I2S2_LRCK		I2S_CODEC_LRCLK_R OUT 46
		AL30	I2S2_MCK		NC_I2S_CODEC_MCLK OUT 46
		R32	I2S3_DIN	(IPD)	NC_I2S_HAWKING_D2R IN 46
		U33	I2S3_DOUT		NC_I2S_CODEC1_R2D_R OUT 46
		T33	I2S3_BCLK		NC_I2S_HAWKING_BCLK_R OUT 46
		U29	I2S3_LRCK		NC_I2S_HAWKING_LRCLK OUT 46
		V33	I2S3_MCK		NC_I2S_SPKRAMP_MCLK_R OUT 46

PLACE_NEAR=U3900.AM4:5MM
PLACE_NEAR=U3900.AN3:5MM
PLACE_NEAR=U3900.AP6:5MM

R4171	20	1 2	5%	1/20W	MF	201	SPI_SOCROM_MOSI	OUT 45
R4172	20	1 2	5%	1/20W	MF	201	SPI_SOCROM_CLK	OUT 45
R4173	20	1 2	5%	1/20W	MF	201	SPI_SOCROM_CS_L	OUT 45

BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

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SoC ISP/I2C/UART/SPI/I2S

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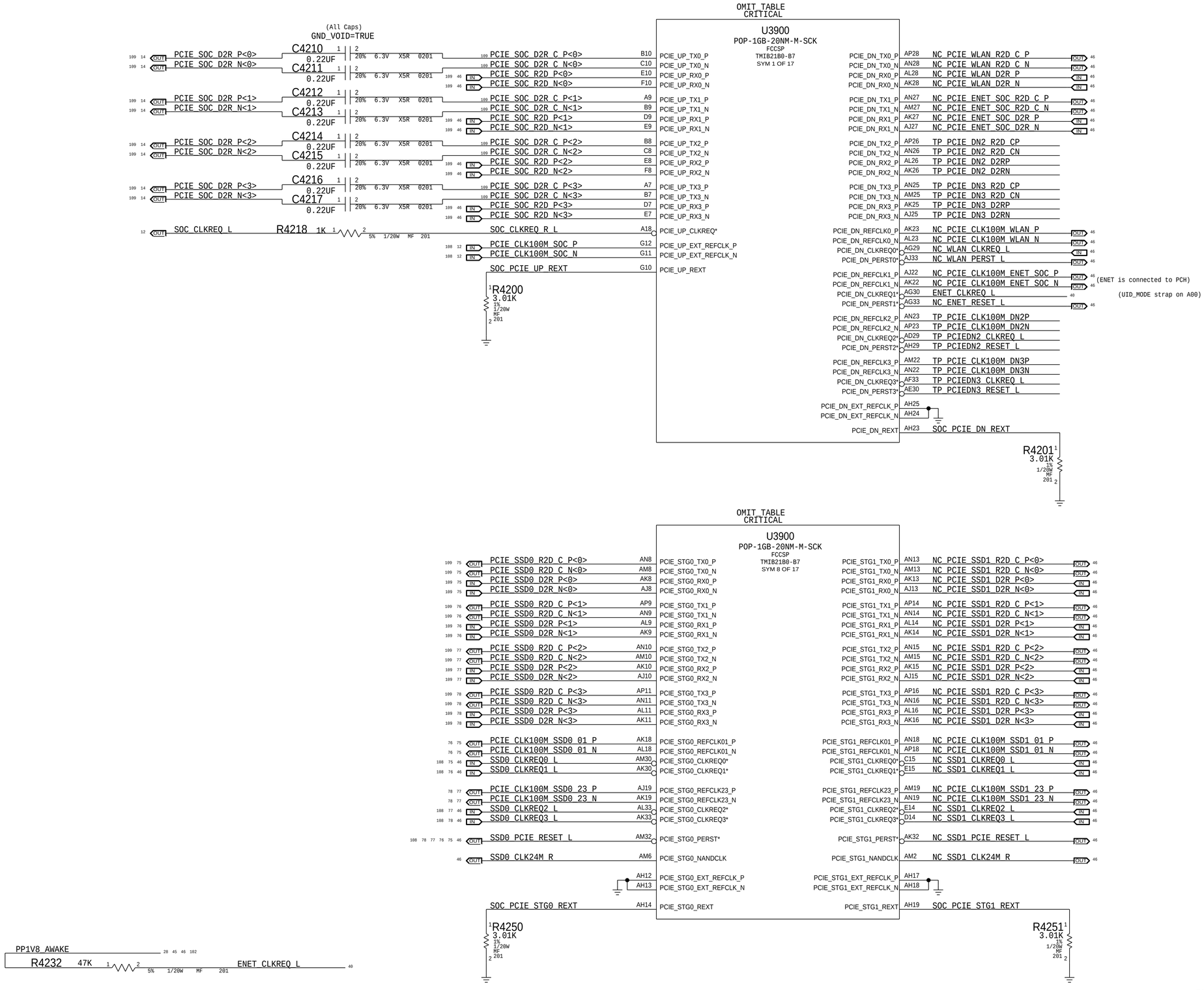

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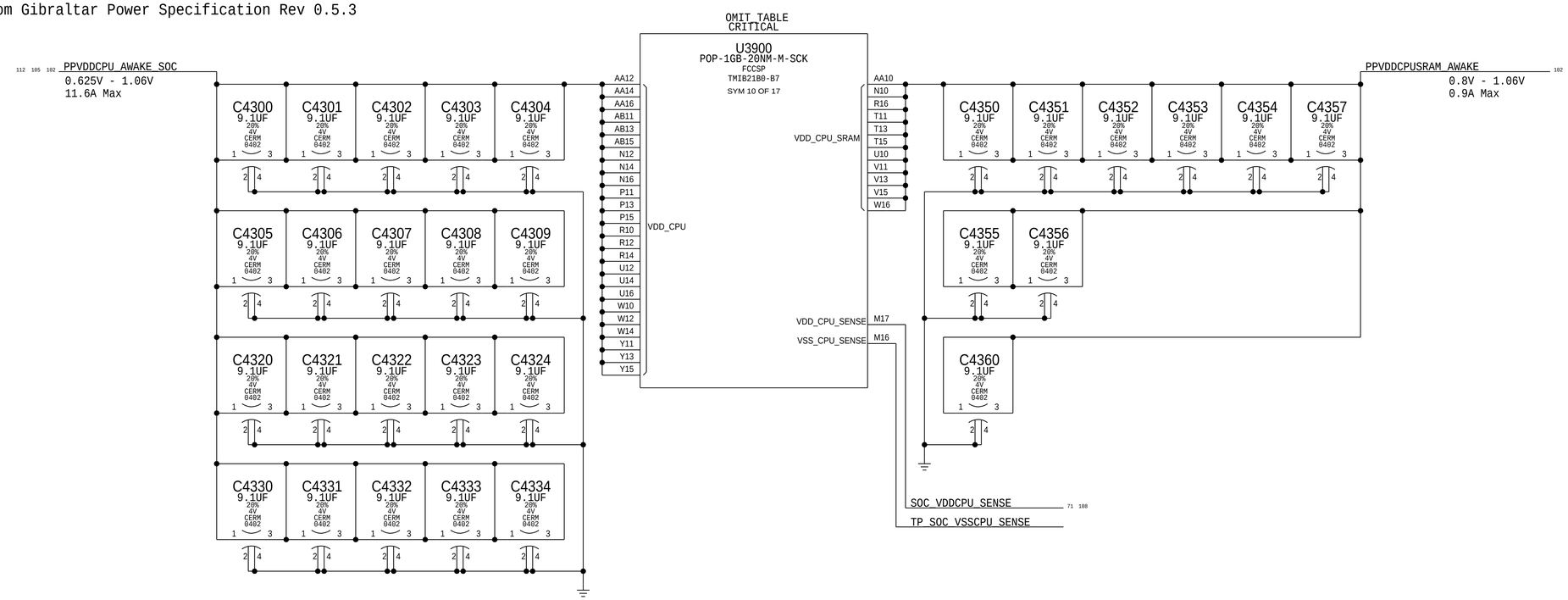

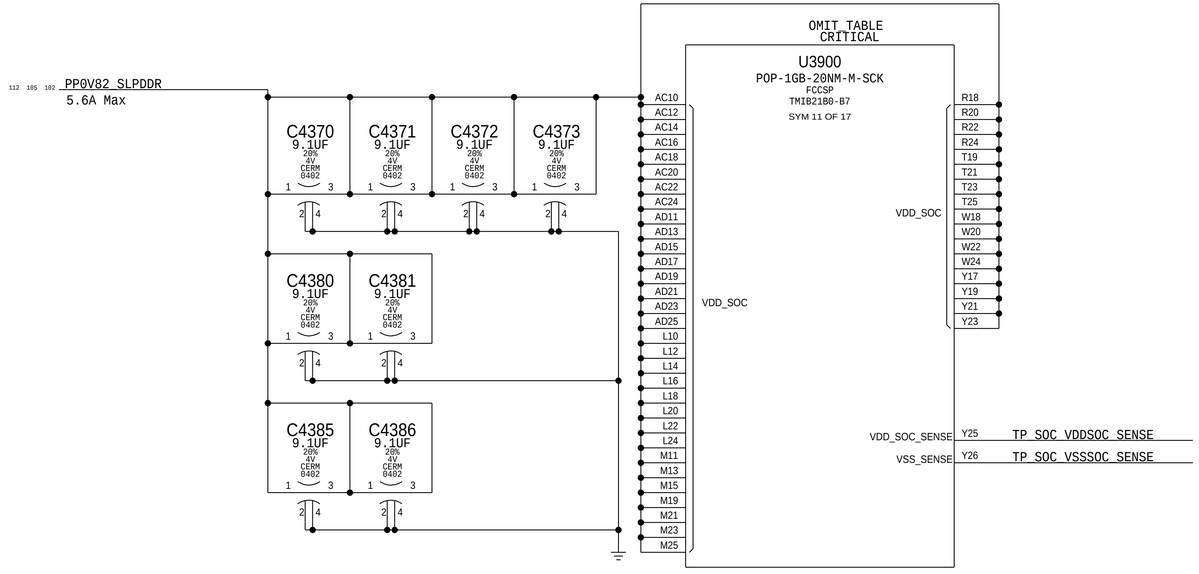

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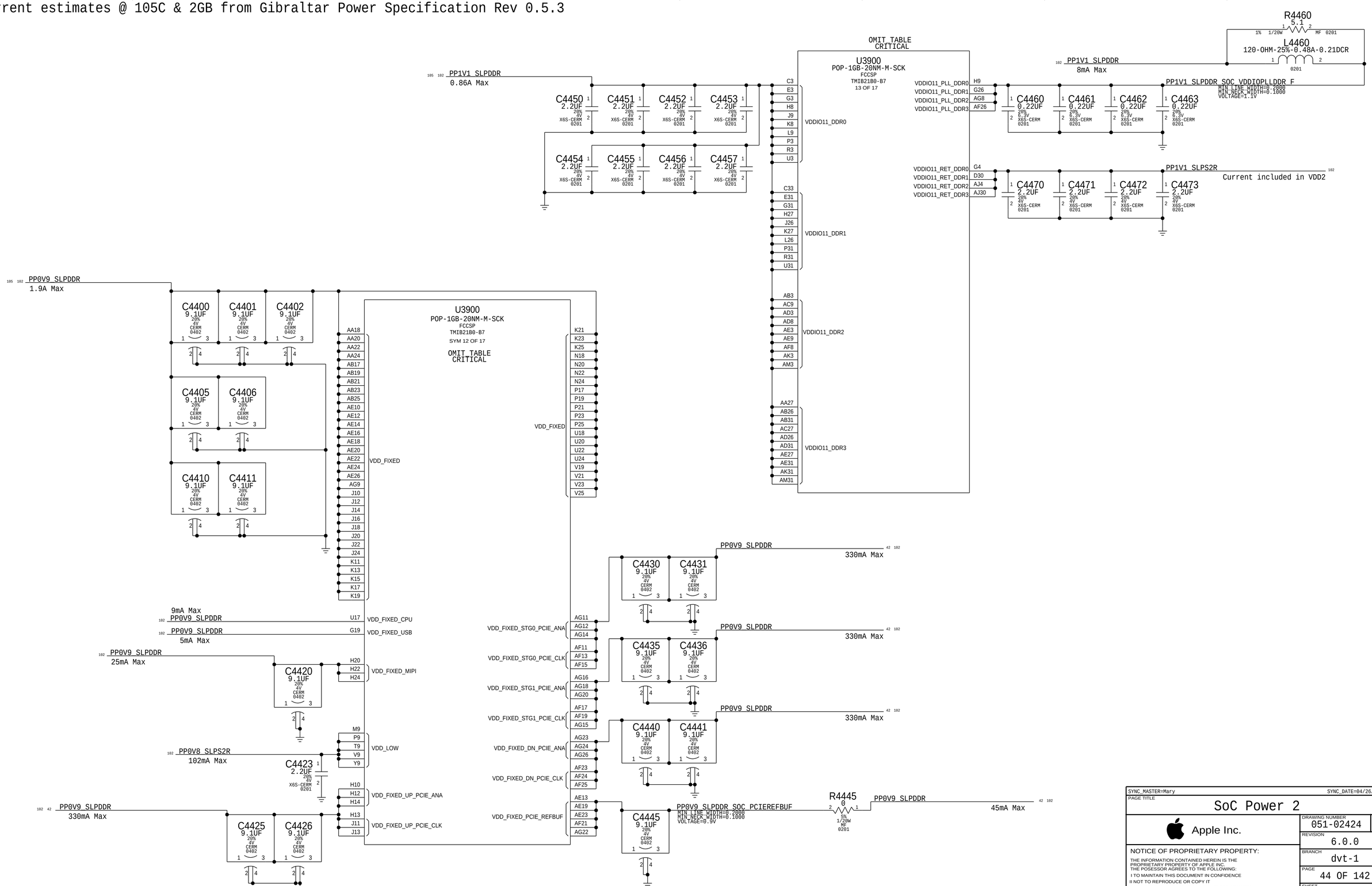

BOM_COST_GROUP=SOC

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SoC Power 2

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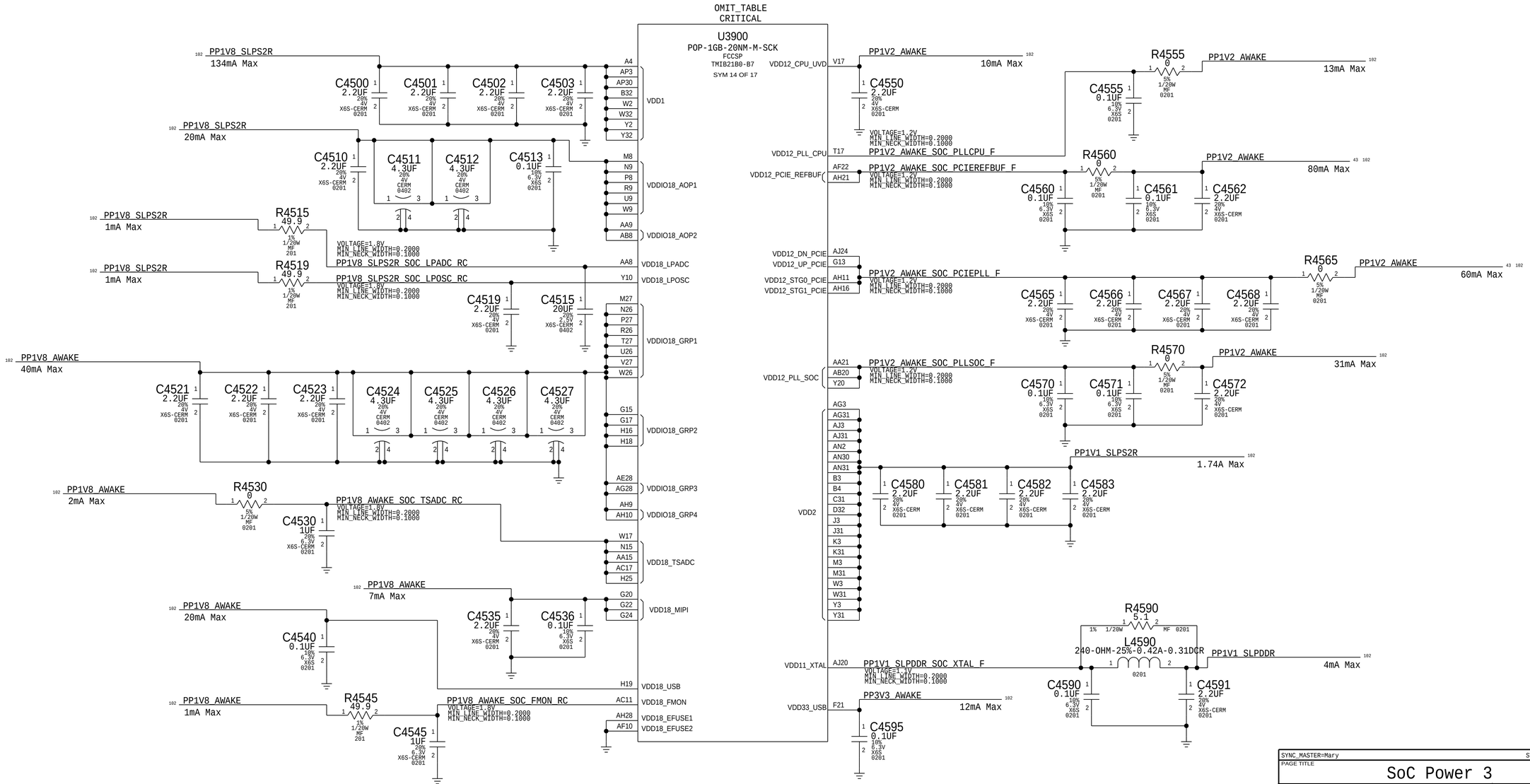
Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3



BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
SoC Power 3

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
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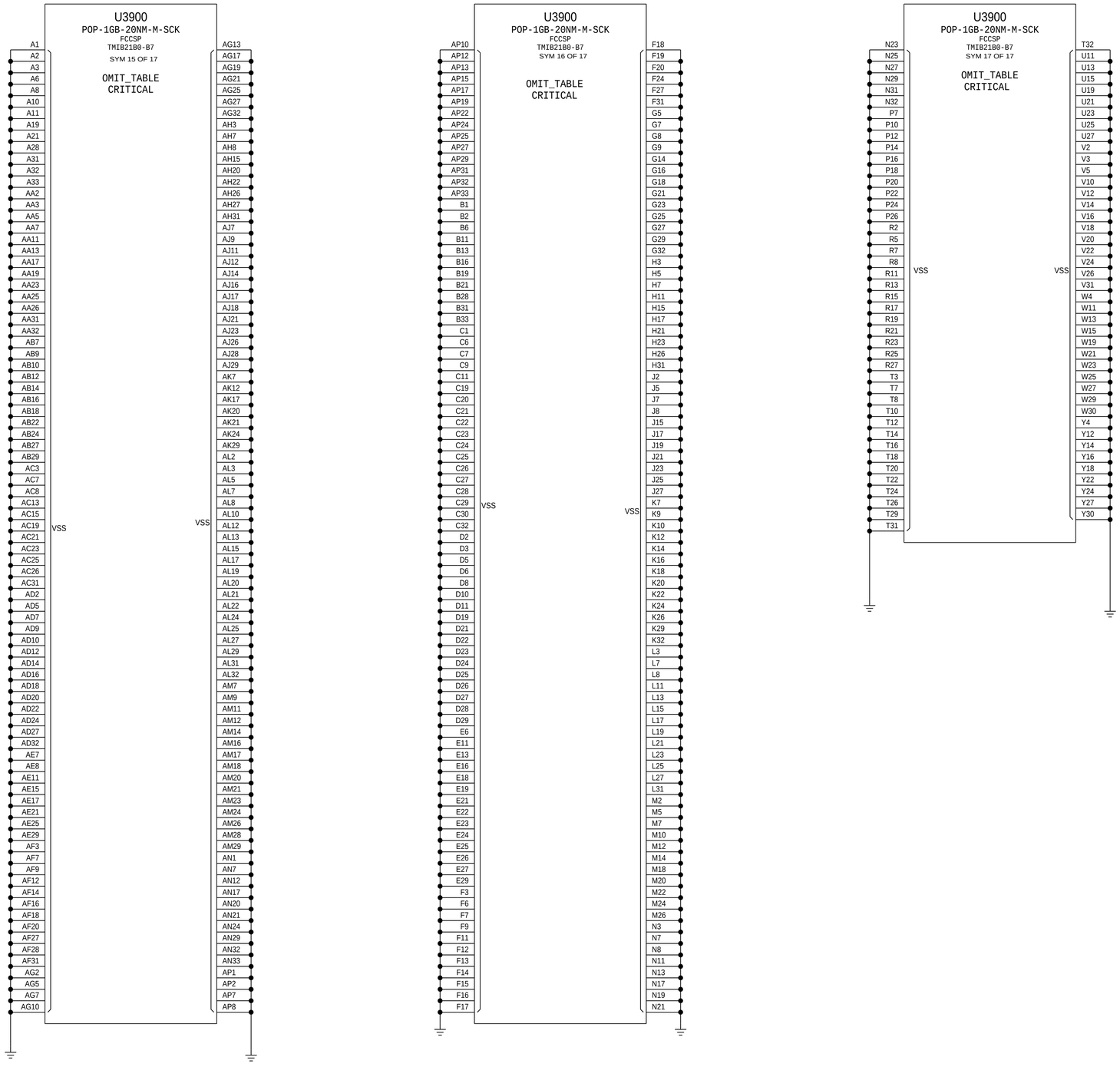

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SYNC_MASTER=Mary SYNC_DATE=04/26/2018

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SoC Ground

Apple Inc.

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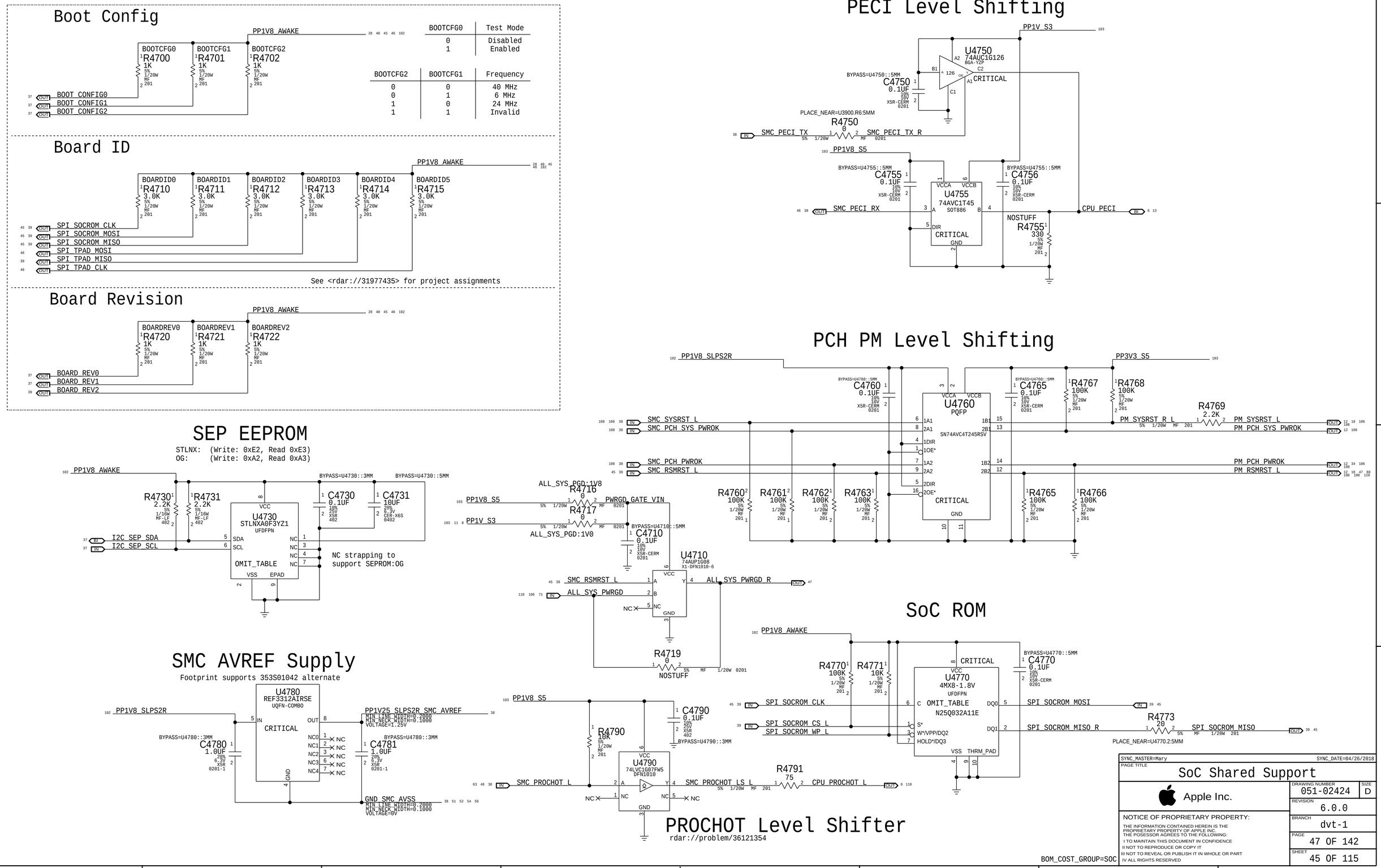
Boot Config
PP1V8_AWAKE
BOOTCFG0 R4700 1K
BOOTCFG1 R4701 1K
BOOTCFG2 R4702 1K
BOOT_CONFIG0
BOOT_CONFIG1
BOOT_CONFIG2
BOOTCFG0 | Test Mode
0 | Disabled
1 | Enabled
BOOTCFG2 | BOOTCFG1 | Frequency
0 | 0 | 40 MHz
0 | 1 | 6 MHz
1 | 0 | 24 MHz
1 | 1 | Invalid
Board ID
PP1V8_AWAKE
BOARDID0 R4710 3.0K
BOARDID1 R4711 3.0K
BOARDID2 R4712 3.0K
BOARDID3 R4713 3.0K
BOARDID4 R4714 3.0K
BOARDID5 R4715 3.0K
SPI_SOCROM_CLK
SPI_SOCROM_MOSI
SPI_SOCROM_MISO
SPI_TPAD_MOSI
SPI_TPAD_MISO
SPI_TPAD_CLK
See <rdar://31977435> for project assignments
Board Revision
PP1V8_AWAKE
BOARDREV0 R4720 1K
BOARDREV1 R4721 1K
BOARDREV2 R4722 1K
BOARD_REV0
BOARD_REV1
BOARD_REV2
SEP EEPROM
STLNX: (Write: 0xE2, Read 0xE3)
OG: (Write: 0xA2, Read 0xA3)
PP1V8_AWAKE
R4730 2.2K
R4731 2.2K
U4730 STLNXA0F3YZ1 UFDFPN
VCC SDA SCL VSS EPAD NC NC NC NC
OMIT_TABLE
BYPASS=U4730::3MM
BYPASS=U4730::5MM
C4730 0.1UF
C4731 10UF
I2C_SEP_SDA
I2C_SEP_SCL
NC strapping to support SEPROM:OG
SMC AVREF Supply
Footprint supports 353S01042 alternate
U4780 REF3312AIRSE UQFN-COMBO
IN OUT NC0 NC1 NC2 NC3 NC4 GND
CRITICAL
PP1V8_SLPS2R
BYPASS=U4780::3MM
C4780 1.0UF
PP1V25_SLPS2R_SMC_AVREF
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.25V
C4781 1.0UF
GND_SMC_AVSS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=0V
PECI Level Shifting
PP1V_S3
U4750 74AUC1G126 8GA-YZP
A2 B1 C2 A1 C1 CRITICAL
BYPASS=U4750::5MM
C4750 0.1UF
PLACE_NEAR=U3900.R6:5MM
R4750 0
SMC_PECI_TX
SMC_PECI_TX_R
PP1V8_S5
BYPASS=U4755::5MM
C4755 0.1UF
U4755 74AVC1T45 SOT886
VCCA VCCB A B DIR GND
CRITICAL
BYPASS=U4755::5MM
C4756 0.1UF
SMC_PECI_RX
CPU_PECI
NOSTUFF
R4755 330
PCH PM Level Shifting
PP1V8_SLPS2R
PP3V3_S5
BYPASS=U4760::5MM
C4760 0.1UF
U4760 PQFP
SN74AVC4T245RSV
VCCA VCCB 1A1 2A1 1DIR 1OE* 1A2 2A2 2DIR 2OE* 1B1 2B1 1B2 2B2 GND
CRITICAL
BYPASS=U4760::5MM
C4765 0.1UF
R4767 100K
R4768 100K
R4769 2.2K
SMC_SYSRST_L
SMC_PCH_SYS_PWROK
SMC_PCH_PWROK
SMC_RSMRST_L
PM_SYSRST_R_L
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PM_RSMRST_L
R4760 100K
R4761 100K
R4762 100K
R4763 100K
R4765 100K
R4766 100K
ALL_SYS_PGD:1V8
R4716 0
R4717 0
PWRGD_GATE_VIN
ALL_SYS_PGD:1V0
PP1V8_S5
PP1V_S3
BYPASS=U4710::5MM
C4710 0.1UF
U4710 74AUP1G08 X1-DFN1010-6
VCC A B GND Y
SMC_RSMRST_L
ALL_SYS_PWRGD
ALL_SYS_PWRGD_R
R4719 0
NOSTUFF
SoC ROM
PP1V8_AWAKE
R4770 100K
R4771 10K
CRITICAL
U4770 4MX8-1.8V UFDFPN
OMIT_TABLE
N25Q032A11E
VCC C S* W*/VPP/DQ2 HOLD*/DQ3 DQ0 DQ1 VSS THRM_PAD
BYPASS=U4770::5MM
C4770 0.1UF
SPI_SOCROM_CLK
SPI_SOCROM_CS_L
SPI_SOCROM_WP_L
SPI_SOCROM_MOSI
SPI_SOCROM_MISO_R
R4773 20
SPI_SOCROM_MISO
PLACE_NEAR=U4770.2:5MM
PP1V8_S5
R4790 10K
C4790 0.1UF
BYPASS=U4790::3MM
U4790 74LVC1G07FW5 DFN1010
VCC A GND Y
SMC_PROCHOT_L
SMC_PROCHOT_LS_L
R4791 75
CPU_PROCHOT_L
PROCHOT Level Shifter
rdar://problem/36121354
BOM_COST_GROUP=SOC
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
SoC Shared Support
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
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SHEET 45 OF 115
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PCIe Up R2D AC Caps

(All Caps)
GND_VOID=TRUE

PCIE SOC R2D C P<0>	C4820	0.22UF	20% 6.3V X5R 0201	PCIE SOC R2D P<0>	PCIE SOC R2D C N<0>	C4821	0.22UF	20% 6.3V X5R 0201	PCIE SOC R2D N<0>
PCIE SOC R2D C P<1>	C4822	0.22UF	20% 6.3V X5R 0201	PCIE SOC R2D P<1>	PCIE SOC R2D C N<1>	C4823	0.22UF	20% 6.3V X5R 0201	PCIE SOC R2D N<1>
PCIE SOC R2D C P<2>	C4824	0.22UF	20% 6.3V X5R 0201	PCIE SOC R2D P<2>	PCIE SOC R2D C N<2>	C4825	0.22UF	20% 6.3V X5R 0201	PCIE SOC R2D N<2>
PCIE SOC R2D C P<3>	C4826	0.22UF	20% 6.3V X5R 0201	PCIE SOC R2D P<3>	PCIE SOC R2D C N<3>	C4827	0.22UF	20% 6.3V X5R 0201	PCIE SOC R2D N<3>

GPIO Source Termination

I2S SPKRAMP R2D R	R4843	33	PLACE_NEAR=U3900.AC32:5MM	5% 1/20W MF 201	I2S SPKRAMP R2D
I2S SPKRAMP BCLK R	R4844	33	PLACE_NEAR=U3900.Y29:5MM	5% 1/20W MF 201	I2S SPKRAMP BCLK
I2S SPKRAMP_LRCLK_R	R4865	33	PLACE_NEAR=U3900.AE32:5MM	5% 1/20W MF 201	I2S_SPKRAMP_LRCLK
I2S CODEC R2D R	R4847	33	PLACE_NEAR=U3900.AA33:5MM	5% 1/20W MF 201	I2S CODEC R2D
I2S CODEC BCLK R	R4848	33	PLACE_NEAR=U3900.AE33:5MM	5% 1/20W MF 201	I2S CODEC BCLK
I2S CODEC D2R	R4863	33	PLACE_NEAR=U3900.Y33:5MM	5% 1/20W MF 201	I2S CODEC D2R RR
I2S CODEC_LRCLK_R	R4864	33	PLACE_NEAR=U3900.V29:5MM	5% 1/20W MF 201	I2S_CODEC_LRCLK
I2S SPKRAMP D2R	R4852	0	PLACE_NEAR=U3900.Y28:5MM	5% 1/20W MF 0201	I2S SPKRAMP D2R RR
SPI TPAD MOSI					SPI TPAD MOSI (MAKE_BASE=TRUE)
SPI TPAD CLK					SPI TPAD CLK (MAKE_BASE=TRUE)
SSD0 CLK24M R	R4857	20	PLACE_NEAR=U3900.AM6:5MM	5% 1/20W MF 201	SSD0 CLK24M

Misc Alias

CODEC INT L	CODEC INT L	
CODEC WAKE L	CODEC WAKE L	MAKE_BASE=TRUE
CODEC RESET L	CODEC RESET L	MAKE_BASE=TRUE
DP2HDMI AOP VDD12ON	DP2HDMI AOP VDD12ON	MAKE_BASE=TRUE
SMC LED ONEWIRE	R4858 0 0201 1/20W 5% MF	SYS LED
TP SMC DEBUG	TP SMC DEBUG	MAKE_BASE=TRUE
PSU11VOC_WAKE_L	PSU11VOC_WAKE_L	
SMC_GFX_THROTTLE_L	SMC_GFX_THROTTLE_L	
LIDINT_L UARTHDD_D2R	LIDINT_L UARTHDD_D2R	
PSU P12V EN L	R4859 0 0201 1/20W 5% MF	SPIHOLD:H9M SPI_DP2HDMI_HOLD
SWD_SOC_SWCLK	R4800 33 5% 1/20W MF 201	DBGMUX_SWD_SOC_CLK
SWD_SOC_SWDIO	R4801 33 5% 1/20W MF 201	DBGMUX_SWD_SOC_IO

MAKE_BASE=TRUE
MAKE_BASE=TRUE
MAKE_BASE=TRUE

Rdar://34600168

PP1V8_SLPS2R
PP1V8_AWAKE

R4883	47K	5% 1/20W MF 201	SSD0_CLKREQ0_L	
R4884	47K	5% 1/20W MF 201	SSD0_CLKREQ1_L	
R4887	47K	5% 1/20W MF 201	SSD0_CLKREQ2_L	
R4888	47K	5% 1/20W MF 201	SSD0_CLKREQ3_L	
R4885	100K	5% 1/20W MF 201	SSD0_PCIE_RESET_L	
R4886	47K	5% 1/20W MF 201	SSD0_CLK24M	
R4889	100K	5% 1/20W MF 201	NC_PDM_DMIC_DATA0	NOSTUFF
R4890	100K	5% 1/20W MF 201	NC_PDM_DMIC_DATA1	NOSTUFF
R4895	100K	5% 1/20W MF 201	SSD_PMU_RESET_L	

R4845	100K	5% 1/20W MF 201	I2S_SPKRAMP_R_R2D_R
R4846	100K	5% 1/20W MF 201	I2S_SPKRAMP_R_BCLK_R
R4866	100K	5% 1/20W MF 201	I2S_SPKRAMP_R_D2R
R4867	100K	5% 1/20W MF 201	I2S_SPKRAMP_R_LRCLK

SMC (Fast) ADC Assignments

P12VIN_V	SMC_P12VIN_VSENSE (MAKE_BASE=TRUE)	SMC_P12VIN_VSENSE
P12VIN_I	SMC_P12VIN_ISENSE (MAKE_BASE=TRUE)	SMC_P12VIN_ISENSE
CPU_HS_I	SMC_CPU_HI_ISENSE (MAKE_BASE=TRUE)	SMC_CPU_HI_ISENSE
CPUCORE_I	SMC_CPU_VCC_ISENSE (MAKE_BASE=TRUE)	SMC_CPU_VCC_ISENSE
CPUCORE_V	SMC_CPU_VCC_VSENSE (MAKE_BASE=TRUE)	SMC_CPU_VCC_VSENSE
CPUGT_V	SMC_CPUGT_VSENSE (MAKE_BASE=TRUE)	SMC_CPUGT_VSENSE
CPUGT_I	SMC_CPUGT_ISENSE (MAKE_BASE=TRUE)	SMC_CPUGT_ISENSE
1V2_S3_I	SMC_P1V2_ISENSE (MAKE_BASE=TRUE)	SMC_P1V2_ISENSE

Calpe (Slow) ADC Assignments

PMU_VDD_I	PMU_P3V3_CAPLE_ISENSE (MAKE_BASE=TRUE)	PMU_P3V3_CAPLE_ISENSE
CPUSA_I	PMU_CPUSA_ISENSE (MAKE_BASE=TRUE)	PMU_CPUSA_ISENSE
DDR2V5_I	PMU_DDR2V5_ISENSE (MAKE_BASE=TRUE)	PMU_DDR2V5_ISENSE
VCCIO_I	PMU_VCCIO_ISENSE (MAKE_BASE=TRUE)	PMU_VCCIO_ISENSE
P5V_G3S_HS_I(12V)	PMU_P5V_G3S_HI_ISENSE (MAKE_BASE=TRUE)	PMU_P5V_G3S_HI_ISENSE
CPUSA_V	PMU_CPUSA_VSENSE (MAKE_BASE=TRUE)	PMU_CPUSA_VSENSE
USBC_5V_I	PMU_P5V_USBC_ISENSE (MAKE_BASE=TRUE)	PMU_P5V_USBC_ISENSE
USBA_5V_I	PMU_P5V_USBA_ISENSE (MAKE_BASE=TRUE)	PMU_P5V_USBA_ISENSE
TBT_3V3_I	PMU_P3V3_TBT_ISENSE (MAKE_BASE=TRUE)	PMU_P3V3_TBT_ISENSE
SSD0_3V3_I	PMU_P3V3_SSD0_ISENSE (MAKE_BASE=TRUE)	PMU_P3V3_SSD0_ISENSE
SSD0_12V_I	PMU_PBUS_SSD0_ISENSE (MAKE_BASE=TRUE)	PMU_PBUS_SSD0_ISENSE
P3V3_G3H_HS_I(12V)	PMU_P3V3_G3H_HI_ISENSE (MAKE_BASE=TRUE)	PMU_P3V3_G3H_HI_ISENSE
P3V3_G3S_WLANBT_I	PMU_P3V3_WLANBT_ISENSE (MAKE_BASE=TRUE)	PMU_P3V3_WLANBT_ISENSE
P3V3_ENET_I	PMU_P3V3_ENET_ISENSE (MAKE_BASE=TRUE)	PMU_P3V3_ENET_ISENSE
P12_ENET_I	PMU_P12V_ENET_ISENSE (MAKE_BASE=TRUE)	PMU_P12V_ENET_ISENSE

WLAN connects to PCH

NC_PCIE_WLAN_R2D_C_P	NC_PCIE_WLAN_R2D_C_P
NC_PCIE_WLAN_R2D_C_N	NC_PCIE_WLAN_R2D_C_N
NC_PCIE_WLAN_D2R_P	NC_PCIE_WLAN_D2R_P
NC_PCIE_WLAN_D2R_N	NC_PCIE_WLAN_D2R_N

ENET connects to PCH

NC_PCIE_ENET_SOC_R2D_C_P	NC_PCIE_ENET_SOC_R2D_C_P
NC_PCIE_ENET_SOC_R2D_C_N	NC_PCIE_ENET_SOC_R2D_C_N
NC_PCIE_ENET_SOC_D2R_P	NC_PCIE_ENET_SOC_D2R_P
NC_PCIE_ENET_SOC_D2R_N	NC_PCIE_ENET_SOC_D2R_N

NC_SPKR_ID1	NC_SPKR_ID1
NC_SPKR_ID0	NC_SPKR_ID0
NC_SMC_FAN_1_PWM	NC_SMC_FAN_1_PWM
NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH
NC_WLAN_PERST_L	NC_WLAN_PERST_L
NC_WLAN_CLKREQ_L	NC_WLAN_CLKREQ_L
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	
GND	

No MIPI

NC_ENET_RESET_L	NC_ENET_RESET_L
NC_UART_GNSS_D2R_CTS_L	NC_UART_GNSS_D2R_CTS_L
NC_UART_GNSS_R2D_RTS_L	NC_UART_GNSS_R2D_RTS_L
NC_UART_SE_D2R	NC_UART_SE_D2R
NC_UART_SE_R2D	NC_UART_SE_R2D
NC_UART_SE_D2R_CTS_L	NC_UART_SE_D2R_CTS_L
NC_UART_SE_R2D_RTS_L	NC_UART_SE_R2D_RTS_L
NC_PCIE_CLK100M_WLAN_P	NC_PCIE_CLK100M_WLAN_P
NC_PCIE_CLK100M_WLAN_N	NC_PCIE_CLK100M_WLAN_N
NC_PCIE_CLK100M_ENET_SOC_P	NC_PCIE_CLK100M_ENET_SOC_P
NC_PCIE_CLK100M_ENET_SOC_N	NC_PCIE_CLK100M_ENET_SOC_N
NC_PCIE_CLK100M_SSD1_01_P	NC_PCIE_CLK100M_SSD1_01_P
NC_PCIE_CLK100M_SSD1_01_N	NC_PCIE_CLK100M_SSD1_01_N
NC_PCIE_CLK100M_SSD1_23_P	NC_PCIE_CLK100M_SSD1_23_P
NC_PCIE_CLK100M_SSD1_23_N	NC_PCIE_CLK100M_SSD1_23_N
NC_SSD1_CLKREQ0_L	NC_SSD1_CLKREQ0_L
NC_SSD1_CLKREQ1_L	NC_SSD1_CLKREQ1_L
NC_SSD1_CLKREQ2_L	NC_SSD1_CLKREQ2_L
NC_SSD1_CLKREQ3_L	NC_SSD1_CLKREQ3_L
NC_SSD1_PCIE_RESET_L	NC_SSD1_PCIE_RESET_L
NC_SSD1_CLK24M_R	NC_SSD1_CLK24M_R
NC_DFR_TOUCH_RSVD	NC_DFR_TOUCH_RSVD

(WIFI is connected to PCH)
(ENET is connected to PCH)

No SSD on Port 1

SoC NC Pins

	NC_PLCAM_TX_THROTTLE	NC_PLCAM_TX_THROTTLE
	NC_GNSS_HOST_TIME	NC_GNSS_HOST_TIME
	NC_GNSS_DEV_WAKE	NC_GNSS_DEV_WAKE
	NC_SE_CTLR_FW_DWLD	NC_SE_CTLR_FW_DWLD
	NC_MESA_INT	NC_MESA_INT
	NC_MESA_PWR_EN	NC_MESA_PWR_EN
	NC_WLAN_DEV_WAKE	NC_WLAN_DEV_WAKE
	NC_TPAD_SPI_EN	NC_TPAD_SPI_EN
	NC_SE_DEV_WAKE	NC_SE_DEV_WAKE
	NC_DFR_DISP_INT	NC_DFR_DISP_INT
	NC_DFR_PWR_EN	NC_DFR_PWR_EN
	NC_SEP_CAM_DISABLE_L	NC_SEP_CAM_DISABLE_L
	NC_SEP_DMIC_DISABLE_L	NC_SEP_DMIC_DISABLE_L
	NC_SEP_DISABLE_STROBE	NC_SEP_DISABLE_STROBE
	NC_SPI_DESCRIPTOR_OVERRIDE_L	NC_SPI_DESCRIPTOR_OVERRIDE_L
	NC_GYRO_INT1	NC_GYRO_INT1
	NC_GYRO_INT2	NC_GYRO_INT2
	NC_SPI_GYRO_CS_L	NC_SPI_GYRO_CS_L
	NC_ALTIMETER_INT	NC_ALTIMETER_INT
	NC_SPI_ALTIMETER_CS_L	NC_SPI_ALTIMETER_CS_L
	NC_I2S_CODEC_MCLK	NC_I2S_CODEC_MCLK
	NC_PDM_DMIC_CLK0_R	NC_PDM_DMIC_CLK0_R
	NC_PDM_DMIC_CLK1_R	NC_PDM_DMIC_CLK1_R
	NC_PLCAM_PROX_INT_L	NC_PLCAM_PROX_INT_L
	NC_PLCAM_ROMEO_B2B_DETECT	NC_PLCAM_ROMEO_B2B_DETECT
	NC_DFR_TOUCH_INT_L	NC_DFR_TOUCH_INT_L
	NC_SMC_GFX_SELF_THROTTLE	NC_SMC_GFX_SELF_THROTTLE
	NC_PDM_DMIC_DATA0	NC_PDM_DMIC_DATA0
	NC_PDM_DMIC_DATA1	NC_PDM_DMIC_DATA1
	NC_SMC_TOPBLK_SWP_L	NC_SMC_TOPBLK_SWP_L
	NC_SPI_AOP_SENSOR_MOSI_R	NC_SPI_AOP_SENSOR_MOSI_R
	NC_SPI_AOP_SENSOR_CLK_R	NC_SPI_AOP_SENSOR_CLK_R
	NC_SPI_AOP_SENSOR_MISO	NC_SPI_AOP_SENSOR_MISO
	NC_PCIE_SSD1_R2D_C_P<0>	NC_PCIE_SSD1_R2D_C_P<0>
	NC_PCIE_SSD1_R2D_C_N<0>	NC_PCIE_SSD1_R2D_C_N<0>
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	NC_PCIE_SSD1_D2R_P<3>	NC_PCIE_SSD1_D2R_P<3>
	NC_PCIE_SSD1_D2R_N<3>	NC_PCIE_SSD1_D2R_N<3>
	NC_SSD1_SWCLK_UART_R2D	NC_SSD1_SWCLK_UART_R2D
	NC_SSD1_SWDIO_UART_D2R	NC_SSD1_SWDIO_UART_D2R
	NC_SPI_MESA_MISO	NC_SPI_MESA_MISO
	NC_SPI_MESA_MOSI_R	NC_SPI_MESA_MOSI_R
	NC_SPI_MESA_CLK_R	NC_SPI_MESA_CLK_R
	NC_SPI_DFR_MISO	NC_SPI_DFR_MISO
	NC_SPI_DFR_MOSI_R	NC_SPI_DFR_MOSI_R
	NC_SPI_DFR_CLK_R	NC_SPI_DFR_CLK_R
	NC_SPI_DFR_CS_L	NC_SPI_DFR_CS_L
	NC_SDCONN_STATE_CHANGE_L	NC_SDCONN_STATE_CHANGE_L
	NC_DFR_TOUCH_RESET_L	NC_DFR_TOUCH_RESET_L
	NC_DFR_TOUCH_CLK32K_RESET_L	NC_DFR_TOUCH_CLK32K_RESET_L
	NC_DFR_DISP_TE	NC_DFR_DISP_TE
	NC_FTCAM_CLK12M_R	NC_FTCAM_CLK12M_R
	NC_FTCAM_RESET_L	NC_FTCAM_RESET_L
	NC_PLCAM_RX_CLK12M_R	NC_PLCAM_RX_CLK12M_R
	NC_PLCAM_RX_RESET_L	NC_PLCAM_RX_RESET_L
	NC_DFR_DISP_RESET_L	NC_DFR_DISP_RESET_L
	NC_PLCAM_TX_CLK12M_R	NC_PLCAM_TX_CLK12M_R
	NC_PLCAM_TX_RESET_L	NC_PLCAM_TX_RESET_L
	NC_PLCAM_TX_INT	NC_PLCAM_TX_INT
	NC_PCHROM_SW_EN	NC_PCHROM_SW_EN
	NC_MESA_MENUKEY_L	NC_MESA_MENUKEY_L
	NC_I2S_HAWKING_D2R	NC_I2S_HAWKING_D2R
	NC_I2S_CODEC1_R2D_R	NC_I2S_CODEC1_R2D_R
	NC_I2S_HAWKING_BCLK_R	NC_I2S_HAWKING_BCLK_R
	NC_I2S_HAWKING_LRCLK	NC_I2S_HAWKING_LRCLK
	NC_I2S_SPKRAMP_MCLK_R	NC_I2S_SPKRAMP_MCLK_R
	NC_SPI_TPAD_CS_L	NC_SPI_TPAD_CS_L
	NC_DISP_GCON_INT_L	NC_DISP_GCON_INT_L

NFC FW downlaod req
T151 Interrupt
NFC/SE device wake
No FaceTime Cam
No Digital Mic
No Altimeter
No GPU
Only for MAF
No Accelerometer
No SSD on Port 1
No GMUX GPIO

MAKE_BASE=TRUE

SMC_PROCHOT_L	P3MM SM1	PP4800
SMC_PECI_RX	P3MM SM1	PP4801

BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
SoC Project Support

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
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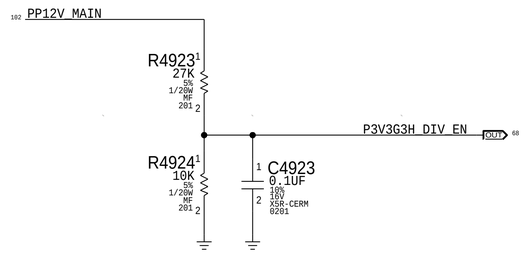
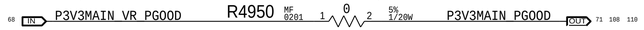
G3H

12V_G3H uses ACDC

3V3_G3H is enabled by PMIC.PVDDMAIN_EN - this is only applied for laptop Big current G3H.
On desktop,3V3_G3H should be enabled by 12V.

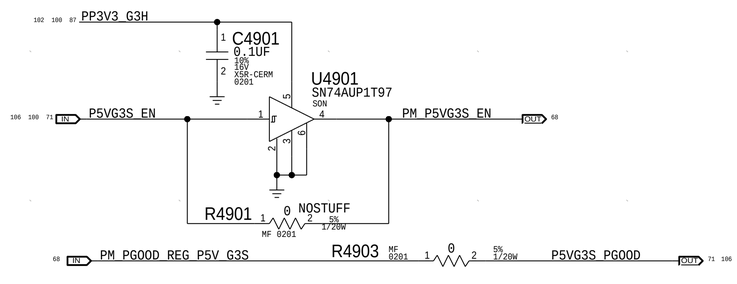


3V3_G3H_PGOOD is to PMIC.GPIO

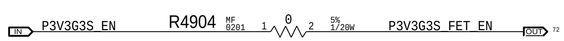


G3S - static timing by PMU

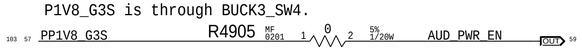
P5V_G3S is enabled by PMIC.GPIO



P3V3_G3S is enabled by PMIC.GPIO



P1V8_G3S is through BUCK3_SW4.



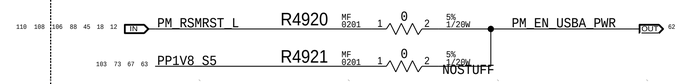
S5 - static timing by PMU

3V3_S5 uses PMU SW

1V8_S5 uses PMU SW

1V05_S5 uses PMU SW

USB-A - HW sequencing

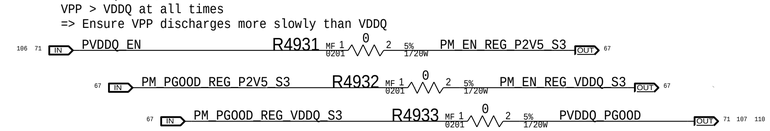


S3

1V2_S3 sequencing

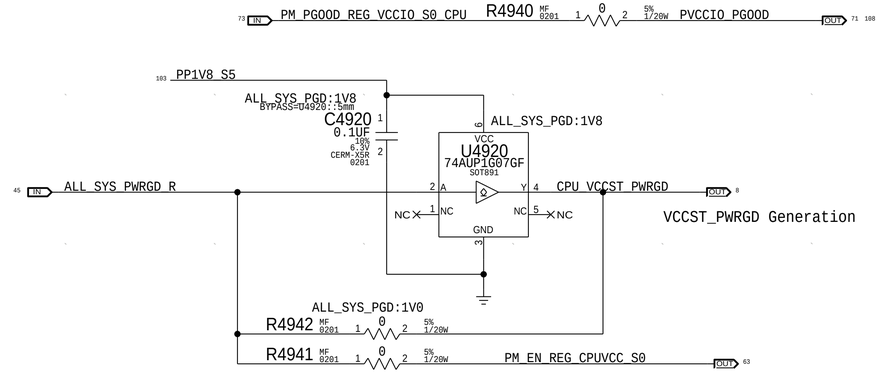
Calpe VDDQ_EN -> 2V5_VTT -> 2V5_PGOOD -> Enable 1V2 VDDQ -> VDDQ_PGDDD

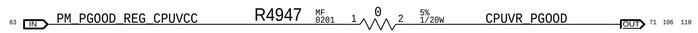
DDR4 Requirement:
VPP > VDDQ at all times
=> Ensure VPP discharges more slowly than VDDQ

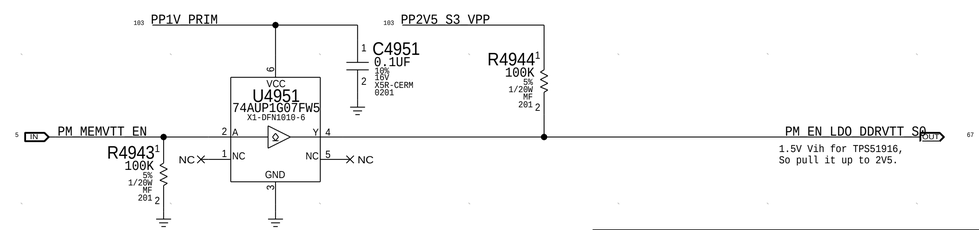


1V05_S3 uses PMU SW

S0 CPU - HW + PMU sequencing







BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
Power Sequencing

Apple Inc.

DRAWING NUMBER 051-02424
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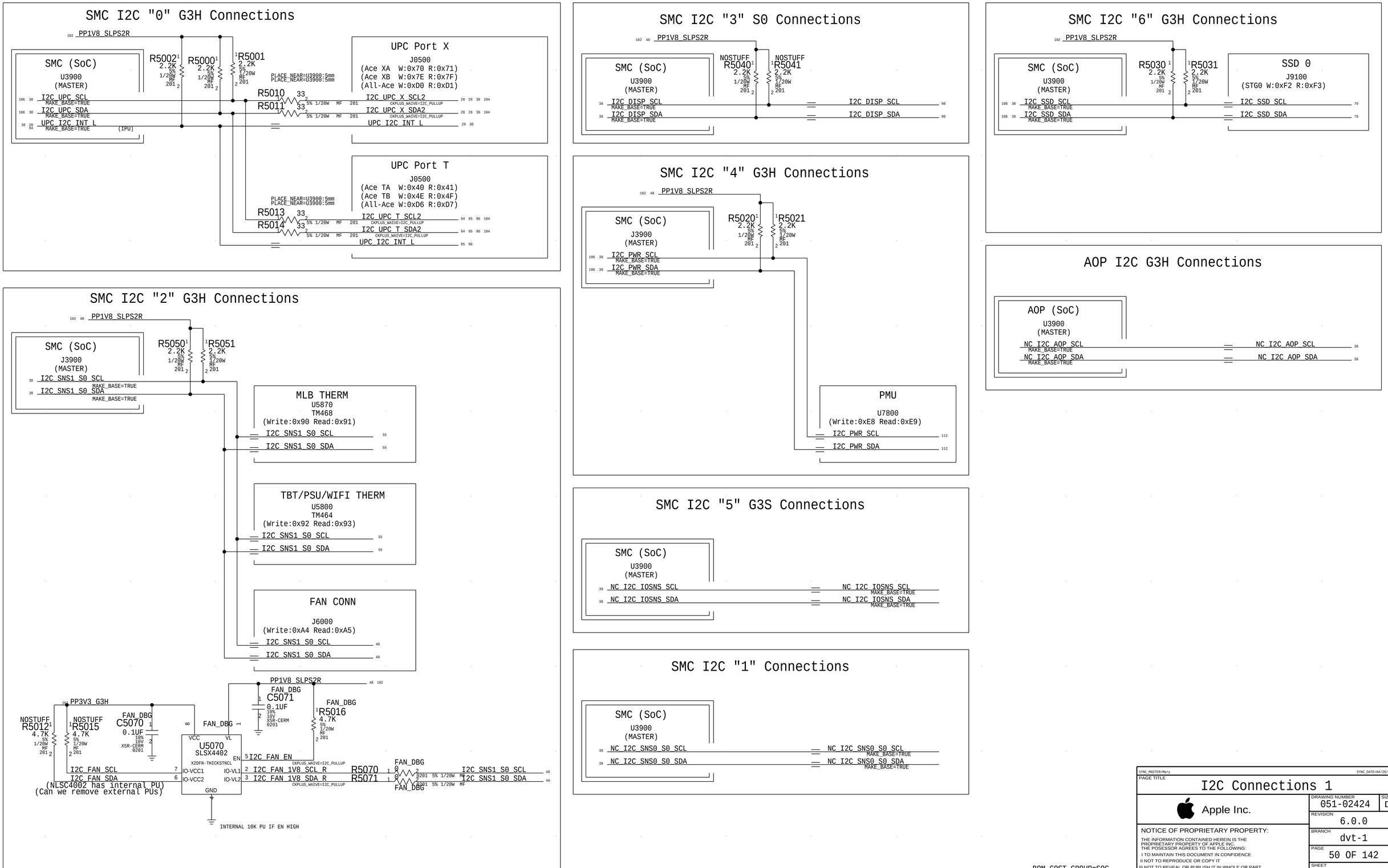

BOM_COST_GROUP=SOC

SYNC_MASTER:Mary SYNC_DATE:04/26/2018

PAGE TITLE

I2C Connections 1

Apple Inc.

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REVISION 6.0.0

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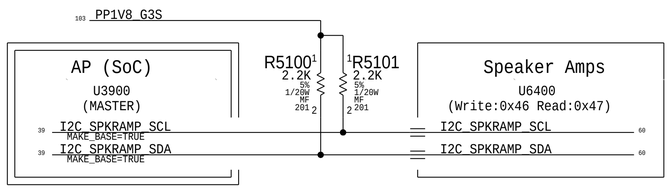
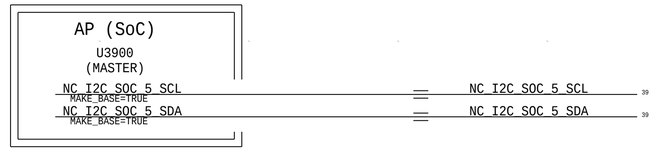
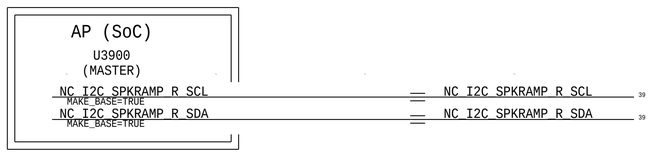
AP I2C "0" G3S Connections



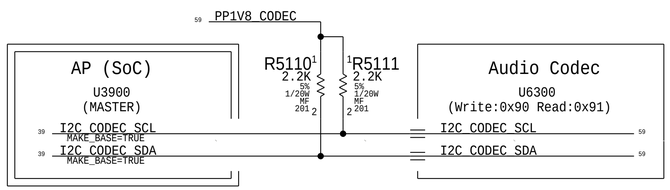
AP I2C "5" Awake Connections



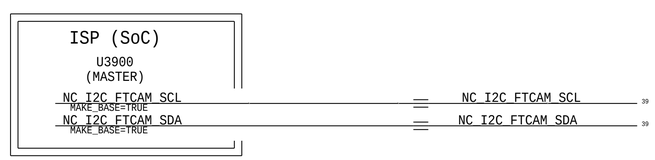
AP I2C "1" G3S Connections



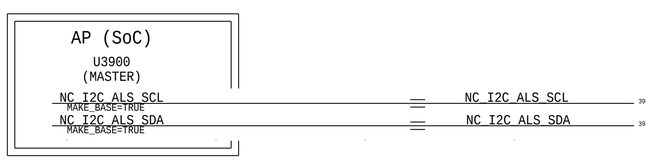
AP I2C "2" Codec Connections



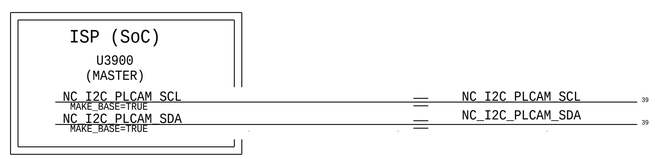
ISP I2C "0" S0 Connections



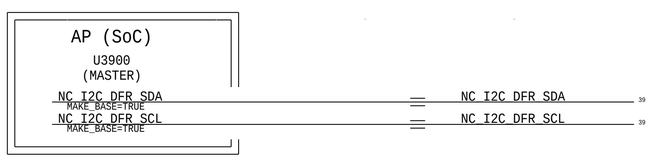
AP I2C "3" S0 Connections



ISP I2C "1" G3S Connections



AP I2C "4" HDMI PCON G3S Connections



BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
I2C Connections 2

Apple Inc.

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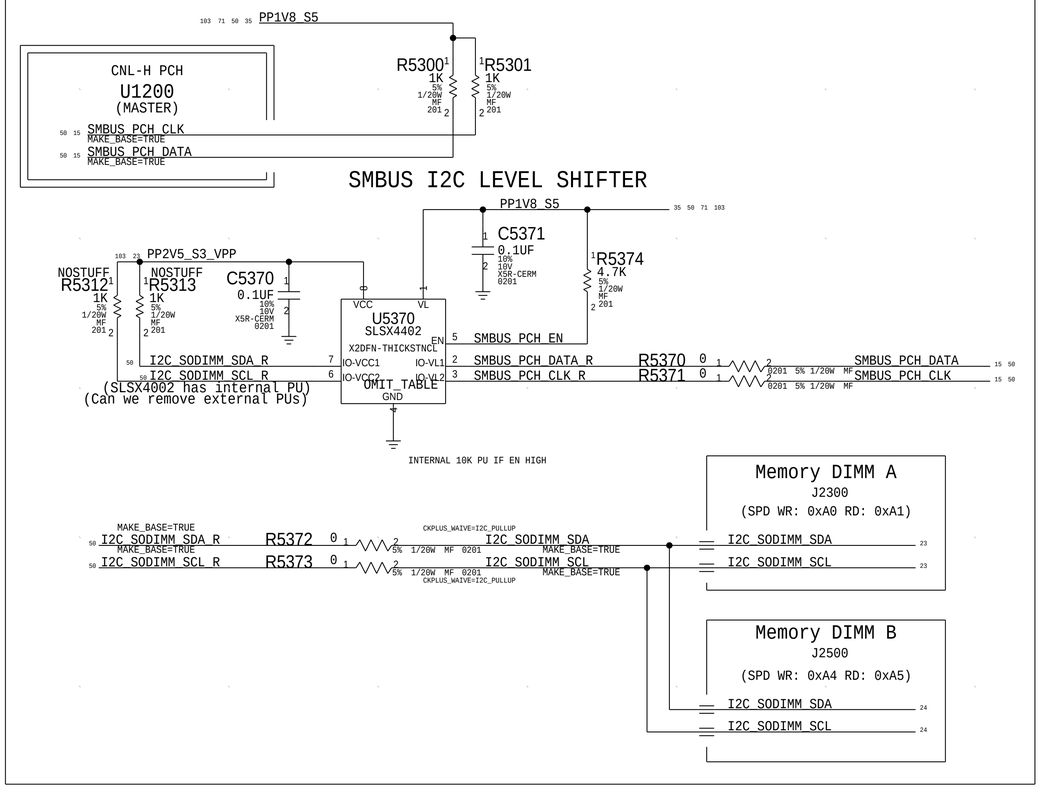
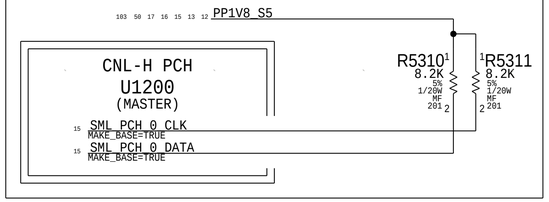
CNL-H PCH "SMBus 0" Connections

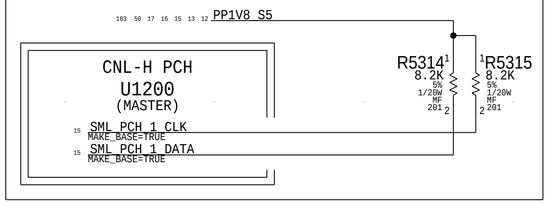


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
311S00179	1	IC,SLSX4402,2BIT D-LVL XLTR,1.8X1.2,DFN8	U5370	CRITICAL	

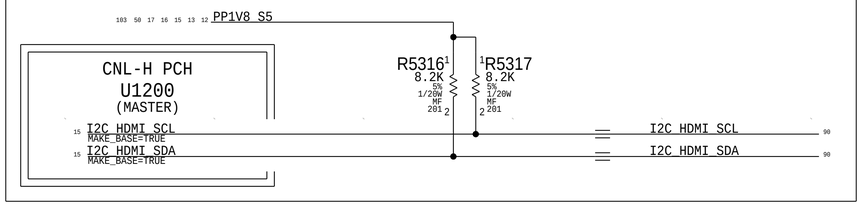
CNL-H PCH "SMLink 0"



CNL-H PCH "SMLink 1"



CNL-H PCH "I2C 0"



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
SMBus Connections

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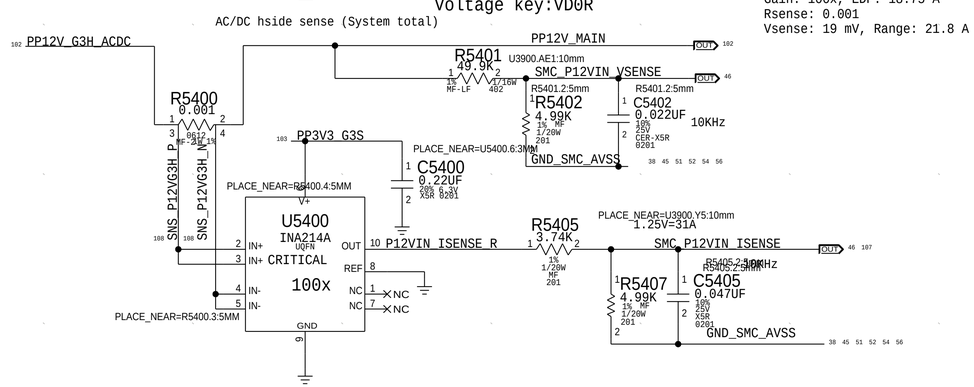
J680 SENSOR SETTINGS

CHIP	Vref(V)	Vmax	SMC sample Freq.	ADR RC filter
H9M	1.25	1.8	10khz	0.1ms
CALPE	1.5	5	10hz	1ms
EADC	2.5	5	1-2hz(10hz)	100ms

PP12V_G3H

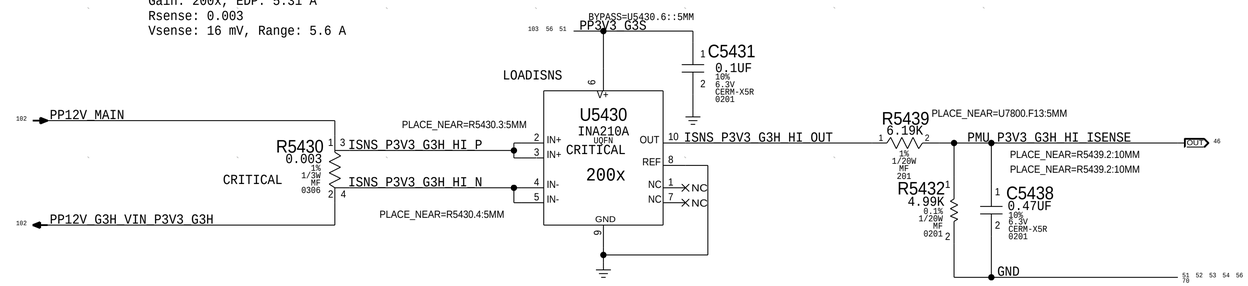
Current key:ID0M
Voltage key:VD0R

Gain: 100x, EDP: 18.75 A
Rsense: 0.001
Vsense: 19 mV, Range: 21.8 A



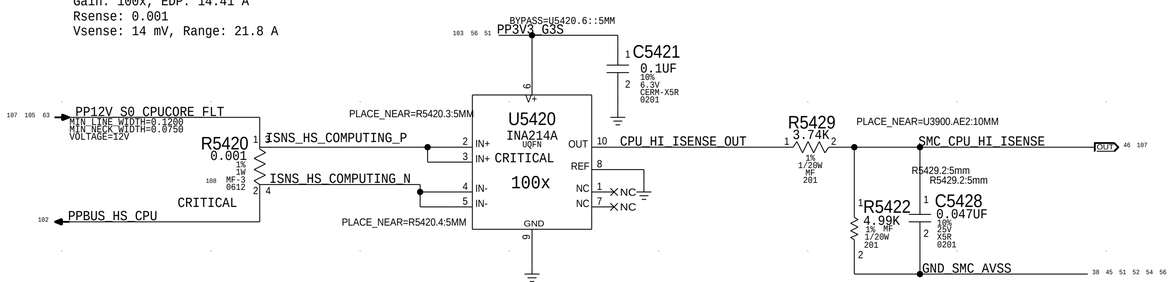
P3V3_G3H High Side Current Sense (IO3R)

Gain: 200x, EDP: 5.31 A
Rsense: 0.003
Vsense: 16 mV, Range: 5.6 A



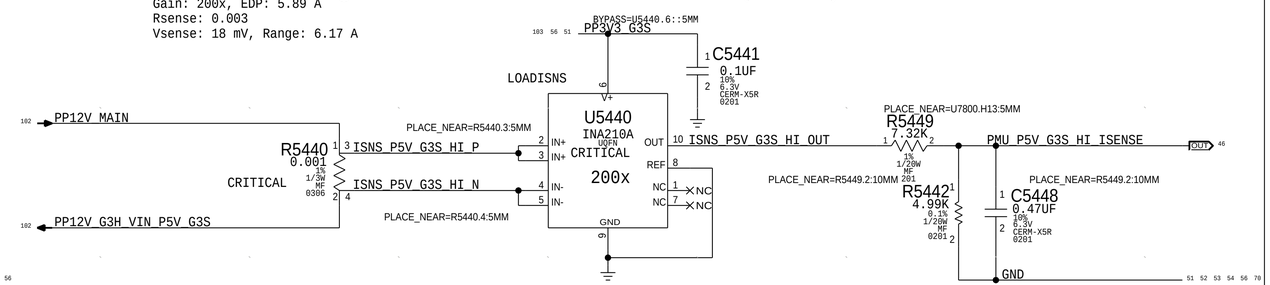
CPU High Side Currrent Sense (IC0R)

Gain: 100x, EDP: 14.41 A
Rsense: 0.001
Vsense: 14 mV, Range: 21.8 A



P5V_G3H High Side Current Sense (IO5R)

Gain: 200x, EDP: 5.89 A
Rsense: 0.003
Vsense: 18 mV, Range: 6.17 A



BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors High Side

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
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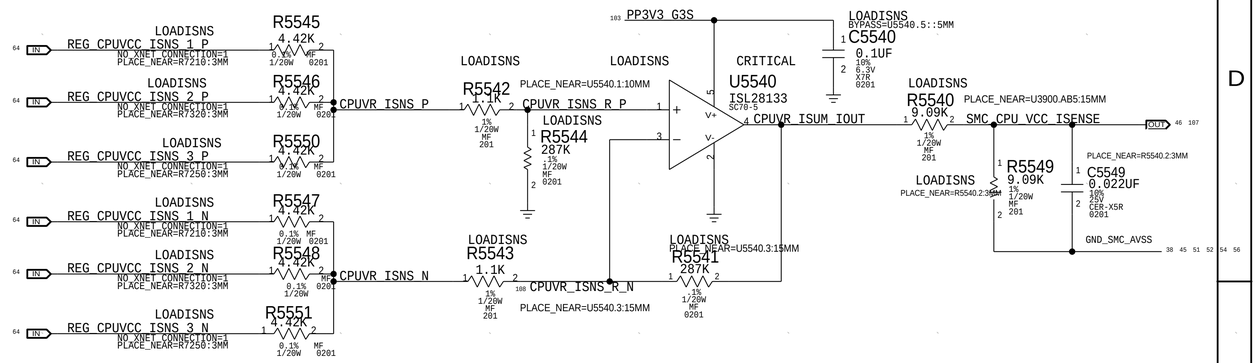
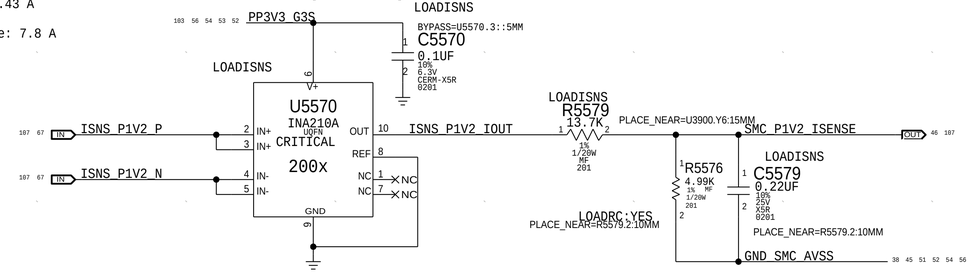
CPU Core Current Sense (ICAC)

Gain: 111.6x, EDP: 128 A
Rsense: 3x of 0.0005
Vsense:22.4 mV, Range: 134.4 A



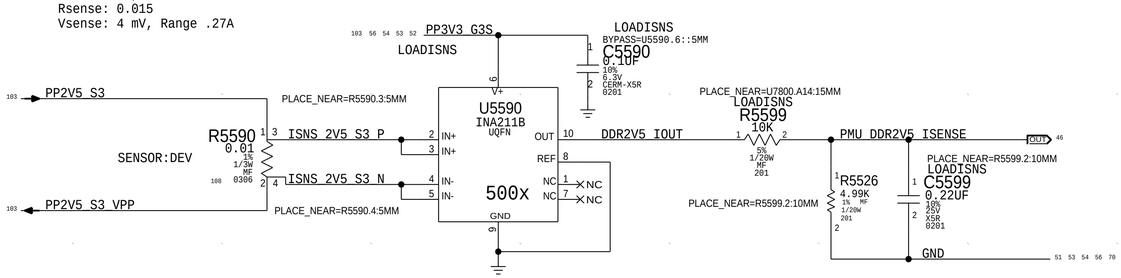
DDR4 1.2V Current Sense (IM0R)

Gain: 200x, EDP: 7.43 A
Rsense: 0.001
Vsense: 7 mV, Range: 7.8 A



2.5V Current Sense (IM0C)

Gain: 500x, EDP: .24 A
Rsense: 0.015
Vsense: 4 mV, Range .27A



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5576,R5519,R5549,C5539,R5529		LOADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors Load Side

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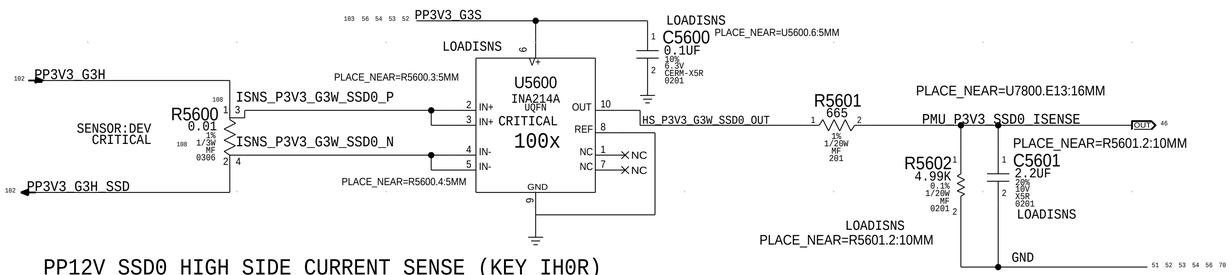
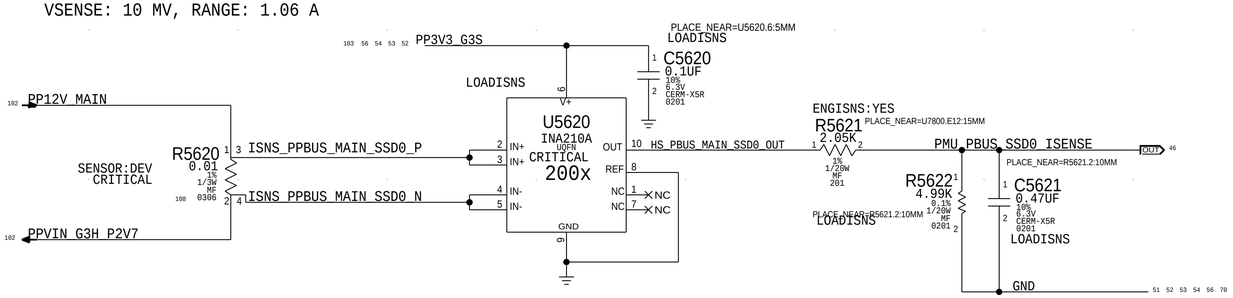
PP3V3_G3W_SSD0 HIGH SIDE CURRENT SENSE (IH0C)

GAIN: 100X, EDP: 1.6 A
RSENSE: 0.01
VSENSE: 16 MV, RANGE: 1.7 A



PP12V_SSD0 HIGH SIDE CURRENT SENSE (KEY IH0R)

GAIN: 200X, EDP: 1 A
RSENSE: 0.01
VSENSE: 10 MV, RANGE: 1.06 A



BOM_COST_GROUP=SENSORS

PAGE TITLE
Power Sensors Extended 1

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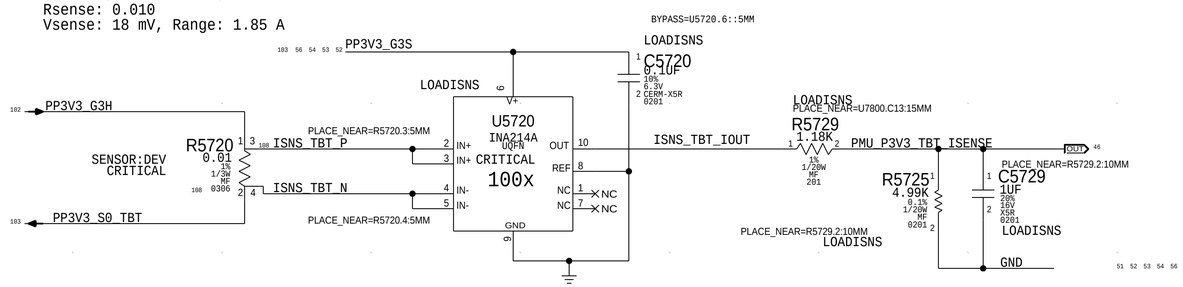
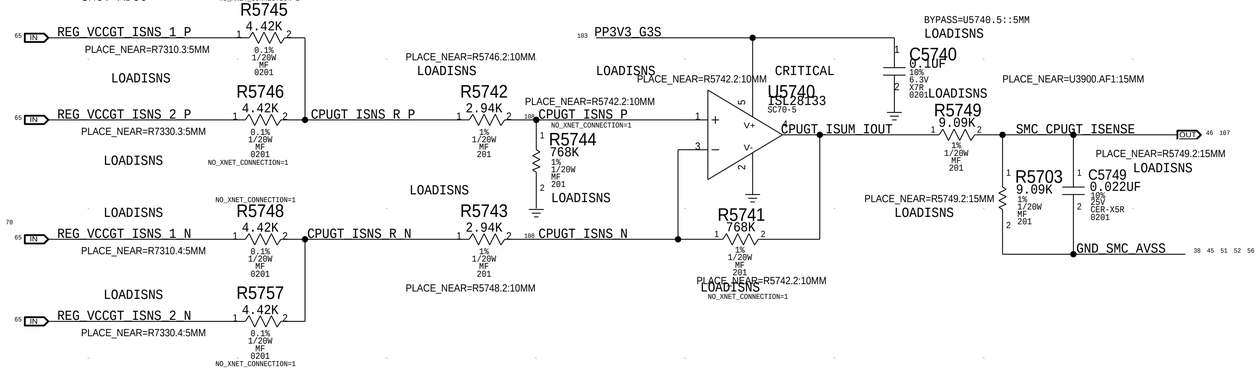
Thunderbolt TBT Current Sense (IU3C)

Gain: 100x. EDP: 1.76 A
Rsense: 0.010
Vsense: 18 mV, Range: 1.85 A



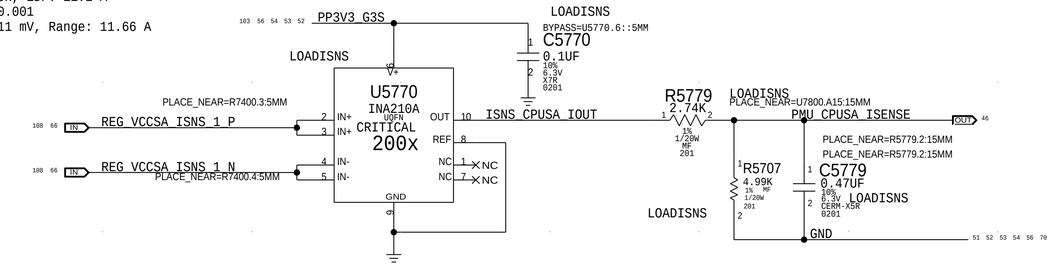
CPU GT Current Sense (ICTC)

Gain: 148.8x, EDP: 32 A
Rsense: 2x of 0.001
Vsense: 16.8 mV, Range:33.6 A
SMC: ADC6



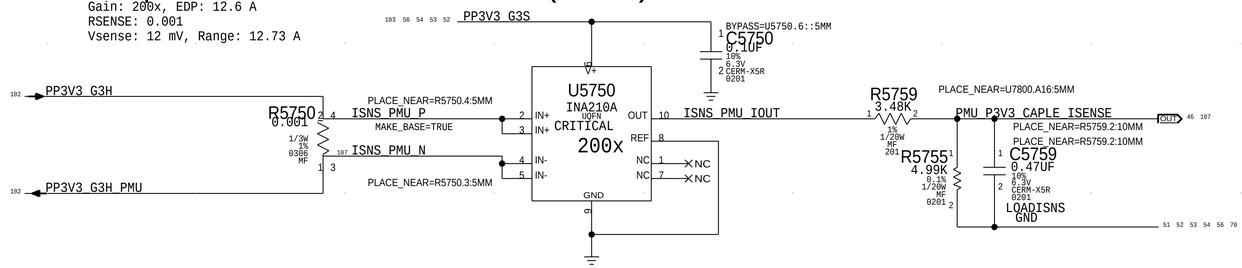
CPU SA Current Sense (ICSC)

Gain: 200x, EDP: 11.1 A
Rsense: 0.001
Vsense: 11 mV, Range: 11.66 A



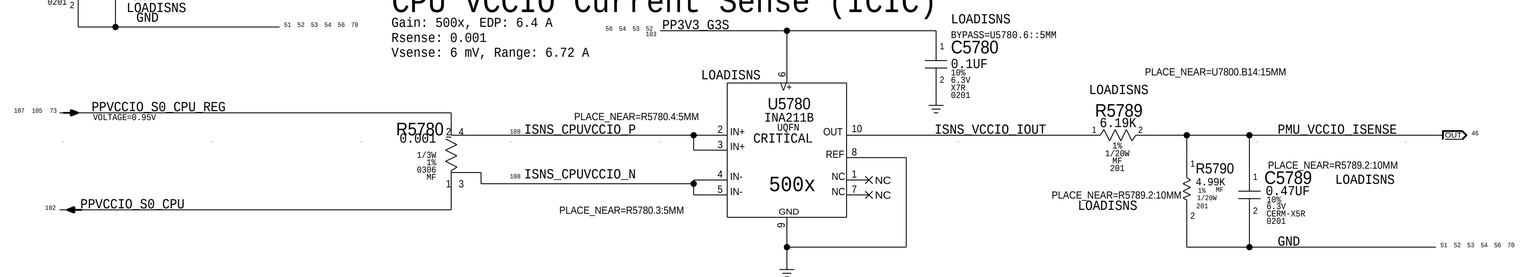
Calpe 3V3 Current Sense (ISLC)

Gain: 200x, EDP: 12.6 A
RSENSE: 0.001
Vsense: 12 mV, Range: 12.73 A



CPU VCCIO Current Sense (ICIC)

Gain: 500x, EDP: 6.4 A
Rsense: 0.001
Vsense: 6 mV, Range: 6.72 A



BOM_COST_GROUP=SENSORS

PAGE TITLE	Power Sensors Extended 2
	Apple Inc.
DRAWING NUMBER	051-02424
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
PAGE	57 OF 142
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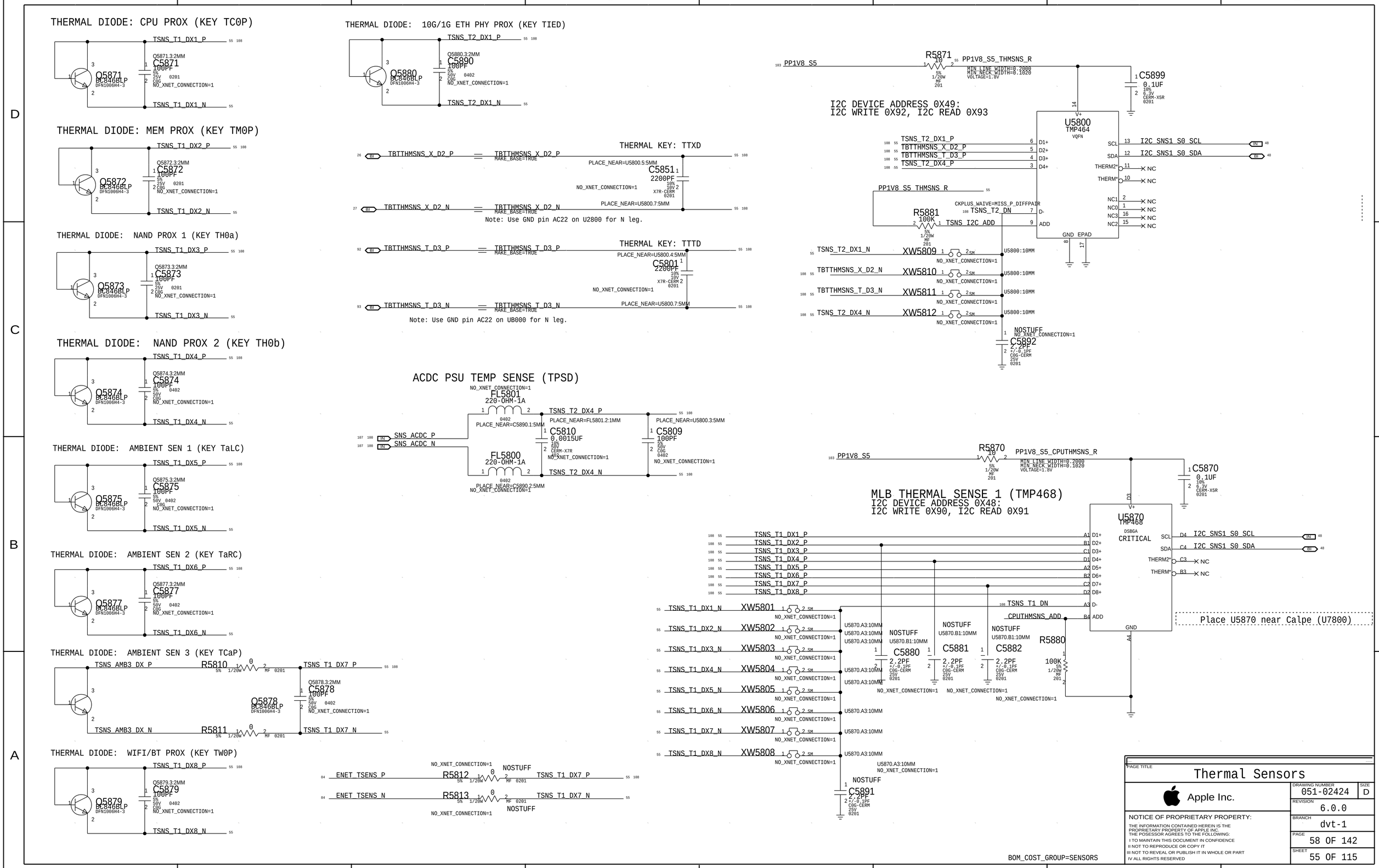
THERMAL DIODE: CPU PROX (KEY TC0P)
TSNS_T1_DX1_P
Q5871 BC846BLP DFN1006H4-3
Q5871:3:2MM C5871 100PF 5% 25V 0201 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX1_N
THERMAL DIODE: 10G/1G ETH PHY PROX (KEY TIED)
TSNS_T2_DX1_P
Q5880 BC846BLP DFN1006H4-3
Q5880:3:2MM C5890 100PF 5% 50V 0402 C0G NO_XNET_CONNECTION=1
TSNS_T2_DX1_N
THERMAL DIODE: MEM PROX (KEY TM0P)
TSNS_T1_DX2_P
Q5872 BC846BLP DFN1006H4-3
Q5872:3:2MM C5872 100PF 5% 25V 0201 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX2_N
THERMAL KEY: TTXD
TBTTHMSNS_X_D2_P
TBTTHMSNS_X_D2_P MAKE_BASE=TRUE
PLACE_NEAR=U5800.5:5MM
C5851 2200PF 10% 10V X7R-CERM 0201
NO_XNET_CONNECTION=1
TBTTHMSNS_X_D2_N
TBTTHMSNS_X_D2_N MAKE_BASE=TRUE
PLACE_NEAR=U5800.7:5MM
Note: Use GND pin AC22 on U2800 for N leg.
THERMAL DIODE: NAND PROX 1 (KEY TH0a)
TSNS_T1_DX3_P
Q5873 BC846BLP DFN1006H4-3
Q5873:3:2MM C5873 100PF 5% 25V 0201 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX3_N
THERMAL KEY: TTTD
TBTTHMSNS_T_D3_P
TBTTHMSNS_T_D3_P MAKE_BASE=TRUE
PLACE_NEAR=U5800.4:5MM
C5801 2200PF 10% 10V X7R-CERM 0201
NO_XNET_CONNECTION=1
TBTTHMSNS_T_D3_N
TBTTHMSNS_T_D3_N MAKE_BASE=TRUE
PLACE_NEAR=U5800.7:5MM
Note: Use GND pin AC22 on UB000 for N leg.
THERMAL DIODE: NAND PROX 2 (KEY TH0b)
TSNS_T1_DX4_P
Q5874 BC846BLP DFN1006H4-3
Q5874:3:2MM C5874 100PF 5% 50V 0402 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX4_N
ACDC PSU TEMP SENSE (TPSD)
NO_XNET_CONNECTION=1
FL5801 220-OHM-1A 0402
PLACE_NEAR=C5890.1:5MM
TSNS_T2_DX4_P
PLACE_NEAR=FL5801.2:1MM
PLACE_NEAR=U5800.3:5MM
C5810 0.0015UF 10% 50V CERM-X7R 0402 NO_XNET_CONNECTION=1
C5809 100PF 5% 50V C0G 0402 NO_XNET_CONNECTION=1
SNS_ACDC_P
SNS_ACDC_N
FL5800 220-OHM-1A 0402
TSNS_T2_DX4_N
PLACE_NEAR=C5890.2:5MM
NO_XNET_CONNECTION=1
THERMAL DIODE: AMBIENT SEN 1 (KEY TaLC)
TSNS_T1_DX5_P
Q5875 BC846BLP DFN1006H4-3
Q5875:3:2MM C5875 100PF 5% 50V 0402 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX5_N
THERMAL DIODE: AMBIENT SEN 2 (KEY TaRC)
TSNS_T1_DX6_P
Q5877 BC846BLP DFN1006H4-3
Q5877:3:2MM C5877 100PF 5% 50V 0402 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX6_N
THERMAL DIODE: AMBIENT SEN 3 (KEY TCaP)
TSNS_AMB3_DX_P
R5810 0 5% 1/20W MF 0201
TSNS_T1_DX7_P
Q5878 BC846BLP DFN1006H4-3
Q5878:3:2MM C5878 100PF 5% 50V 0402 C0G NO_XNET_CONNECTION=1
TSNS_AMB3_DX_N
R5811 0 5% 1/20W MF 0201
TSNS_T1_DX7_N
THERMAL DIODE: WIFI/BT PROX (KEY TW0P)
TSNS_T1_DX8_P
Q5879 BC846BLP DFN1006H4-3
Q5879:3:2MM C5879 100PF 5% 50V 0402 C0G NO_XNET_CONNECTION=1
TSNS_T1_DX8_N
ENET_TSENS_P
R5812 0 5% 1/20W MF 0201 NOSTUFF
ENET_TSENS_N
R5813 0 5% 1/20W MF 0201 NOSTUFF
NO_XNET_CONNECTION=1
PP1V8_S5
R5871 10 5% 1/20W MF 0201
PP1V8_S5_THMSNS_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1020
VOLTAGE=1.8V
C5899 0.1UF 10% 6.3V CERM-X5R 0201
I2C DEVICE ADDRESS 0X49:
I2C WRITE 0X92, I2C READ 0X93
U5800 TMP464 VQFN
TSNS_T2_DX1_P
TBTTHMSNS_X_D2_P
TBTTHMSNS_T_D3_P
TSNS_T2_DX4_P
D1+ D2+ D3+ D4+ D-
SCL SDA THERM2* THERM* NC1 NC0 NC3 NC2 ADD GND EPAD
I2C_SNS1_S0_SCL
I2C_SNS1_S0_SDA
NC
PP1V8_S5_THMSNS_R
R5881 100K 5% 1/20W MF 201
CKPLUS_WAIVE=MISS_P_DIFFPAIR
TSNS_T2_DN
TSNS_I2C_ADD
XW5809 XW5810 XW5811 XW5812
U5800:10MM
NO_XNET_CONNECTION=1
NOSTUFF
C5892 2.2PF +/-0.1PF C0G-CERM 25V 0201
PP1V8_S5
R5870 10 5% 1/20W MF 201
PP1V8_S5_CPUTHMSNS_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1020
VOLTAGE=1.8V
C5870 0.1UF 10% 6.3V CERM-X5R 0201
MLB THERMAL SENSE 1 (TMP468)
I2C DEVICE ADDRESS 0X48:
I2C WRITE 0X90, I2C READ 0X91
U5870 TMP468 DSBGA CRITICAL
TSNS_T1_DX1_P
TSNS_T1_DX2_P
TSNS_T1_DX3_P
TSNS_T1_DX4_P
TSNS_T1_DX5_P
TSNS_T1_DX6_P
TSNS_T1_DX7_P
TSNS_T1_DX8_P
D1+ D2+ D3+ D4+ D5+ D6+ D7+ D8+ D- ADD GND
I2C_SNS1_S0_SCL
I2C_SNS1_S0_SDA
NC
TSNS_T1_DN
CPUTHMSNS_ADD
Place U5870 near Calpe (U7800)
XW5801 XW5802 XW5803 XW5804 XW5805 XW5806 XW5807 XW5808
U5870.A3:10MM
U5870.B1:10MM
C5880 2.2PF +/-0.1PF C0G-CERM 25V 0201
C5881 2.2PF +/-0.1PF C0G-CERM 25V 0201
C5882 2.2PF +/-0.1PF C0G-CERM 25V 0201
R5880 100K 5% 1/20W MF 201
C5891 2.2PF +/-0.1PF C0G-CERM 25V 0201
BOM_COST_GROUP=SENSORS
PAGE TITLE
Thermal Sensors
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
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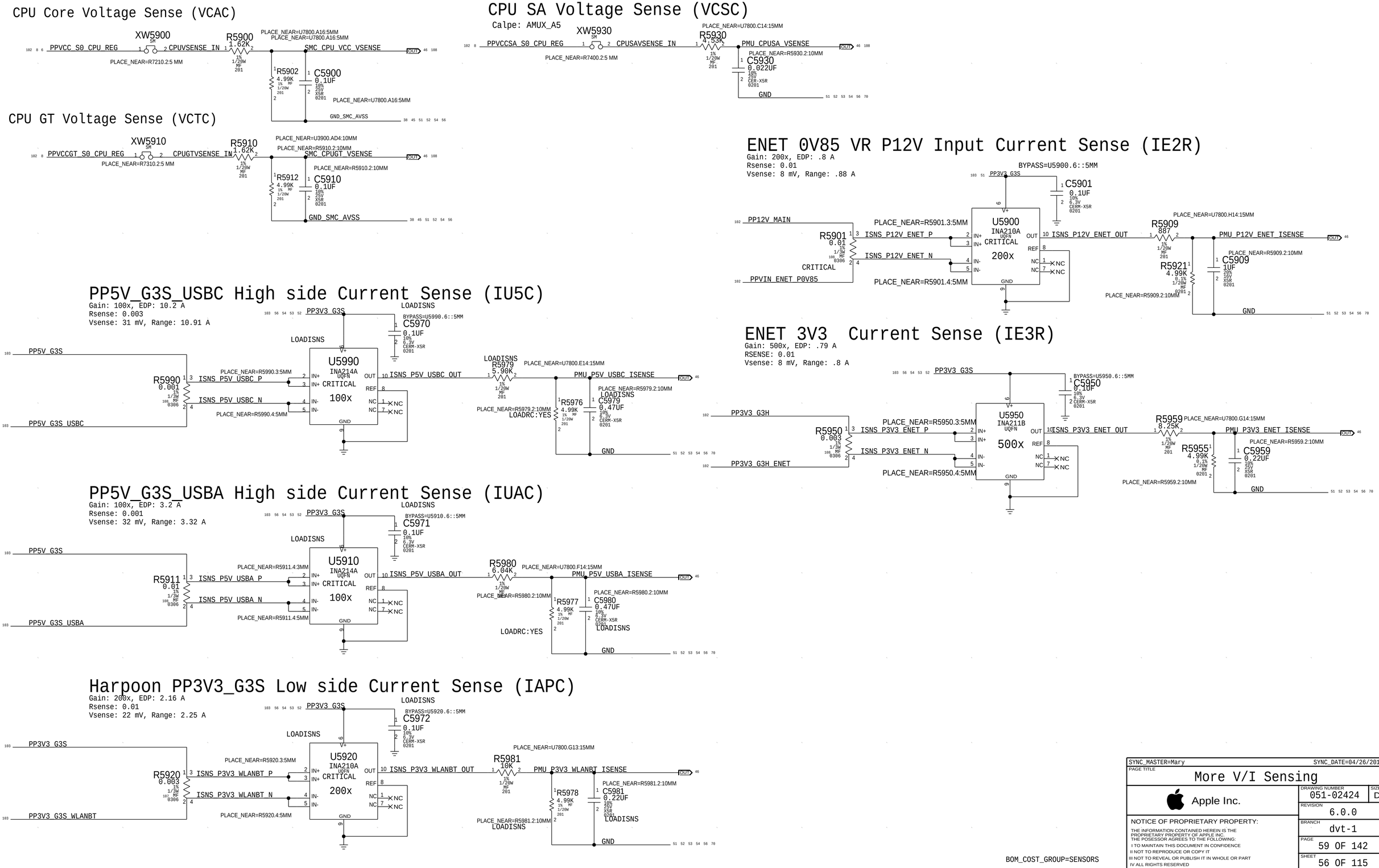

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: More V/I Sensing

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

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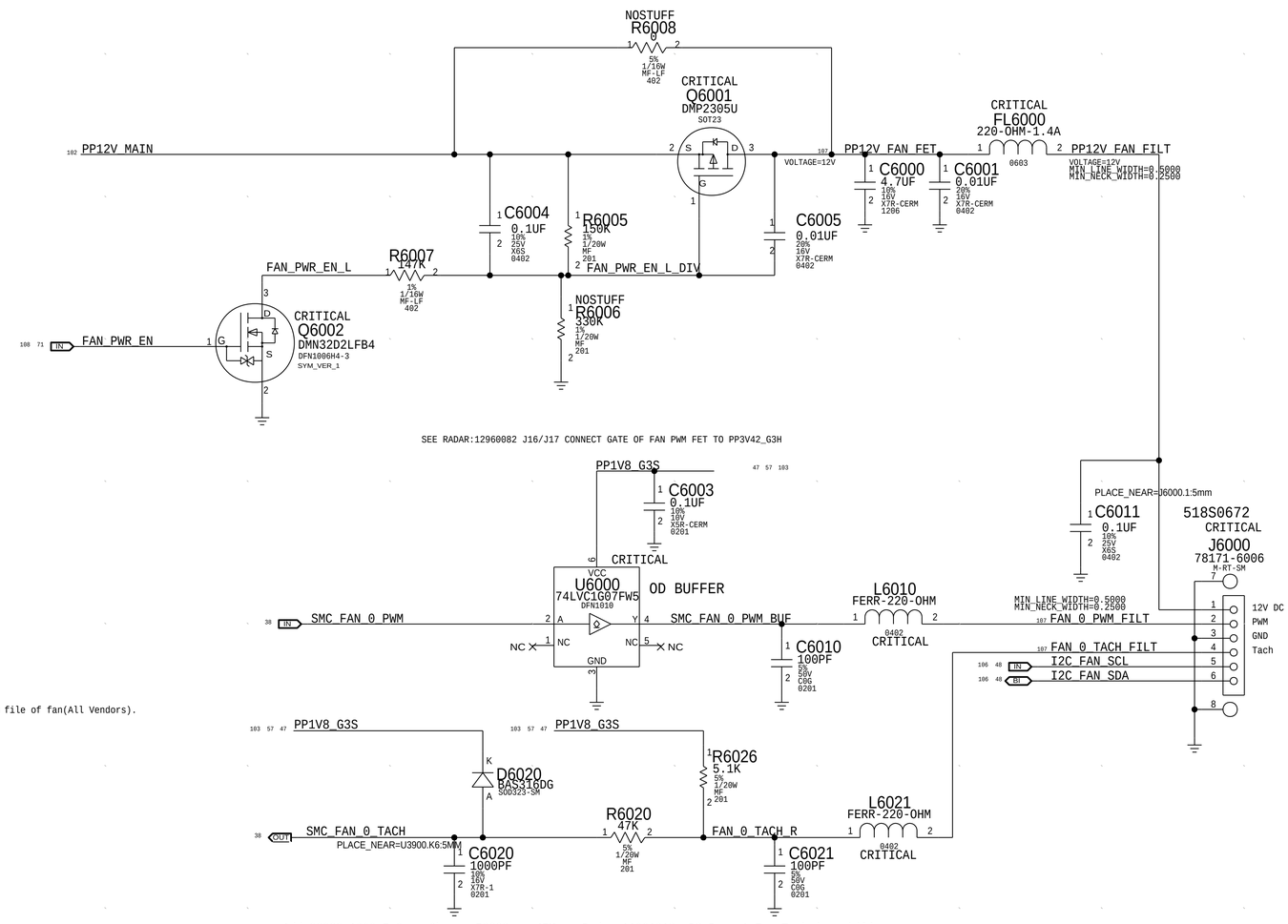
SMC Fan 0 (System)



SEE RADAR:12960082 J16/J17 CONNECT GATE OF FAN PWM FET TO PP3V42_G3H

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).

Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

BOM_COST_GROUP=FAN

SYNC_MASTER=Mary	SYNC_DATE=04/26/2018
PAGE TITLE	System Fan Connector
Apple Inc.	DRAWING NUMBER 051-02424 / SIZE D
	REVISION 6.0.0
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BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

SPI Debug Connector

Apple Inc.

DRAWING NUMBER	051-02424
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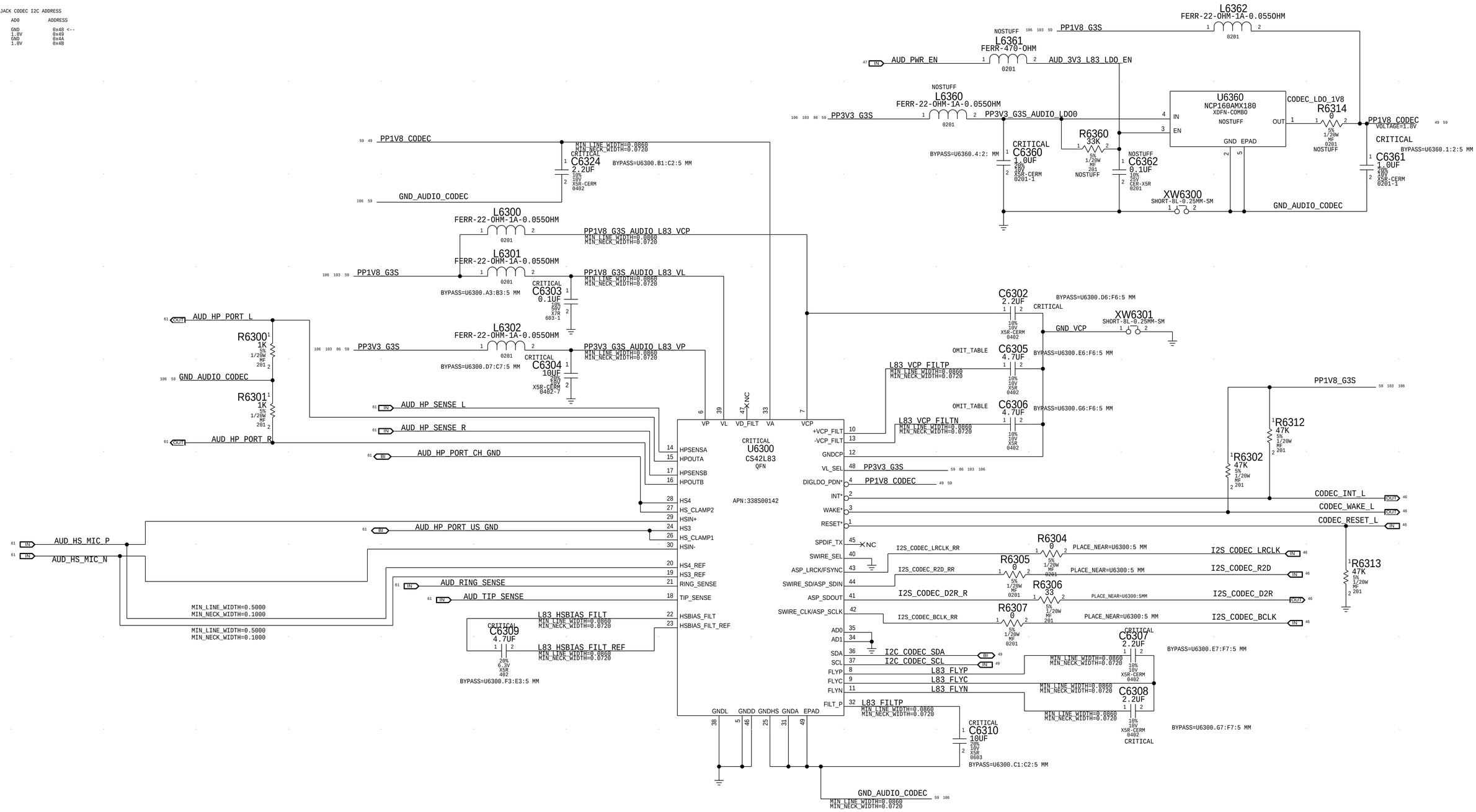
AUDIO JACK CODEC I2C ADDRESS

AD1	AD0	ADDRESS
GND	GND	0x48 <--
GND	1.8V	0x49
1.8V	GND	0x4A
1.8V	1.8V	0x4B



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0719	2	CAP,CER,4.7UF,20%,10V,X5R,0402,MURATA	C6305,C6306	CRITICAL	

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO JACK CODEC

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

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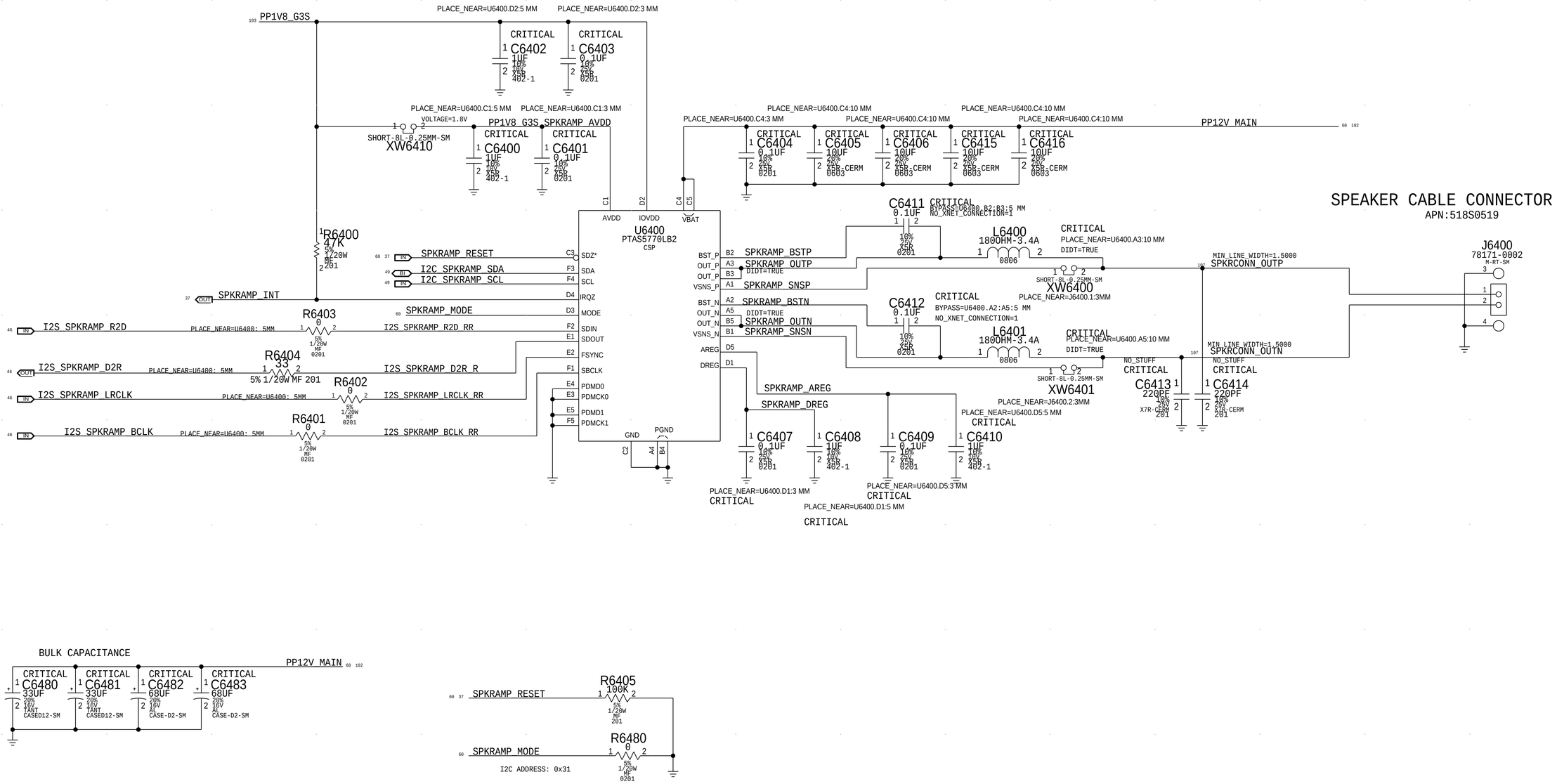
1x MONO SPEAKER AMPLIFIER (TAS5770)

APN: 353S01629



BOM_COST_GROUP=AUDIO

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

AUDIO SKPR AMP

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

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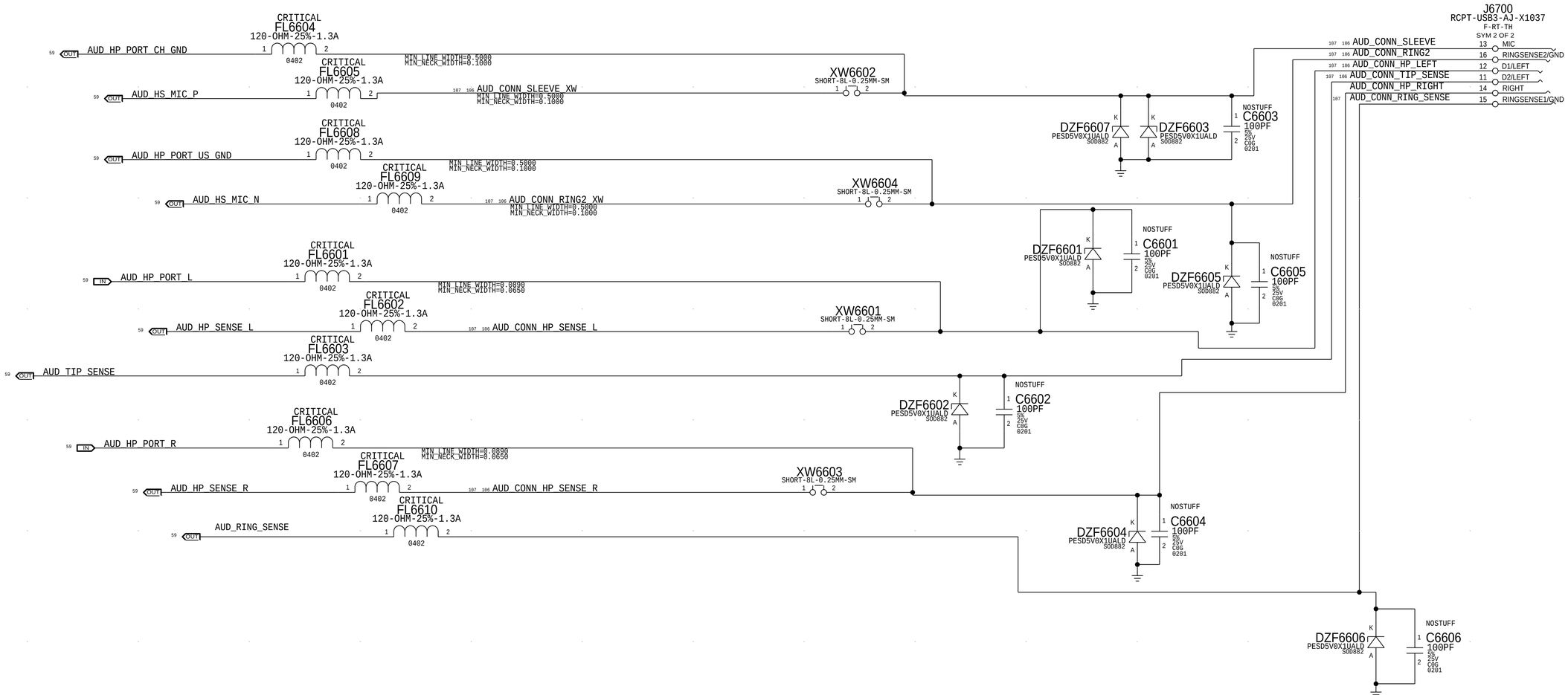

BOM_COST_GROUP=AUDIO

PAGE TITLE

AUDIO JACK CONNECTOR

Apple Inc.

DRAWING NUMBER 051-02424

SIZE D

REVISION 6.0.0

BRANCH dvt-1

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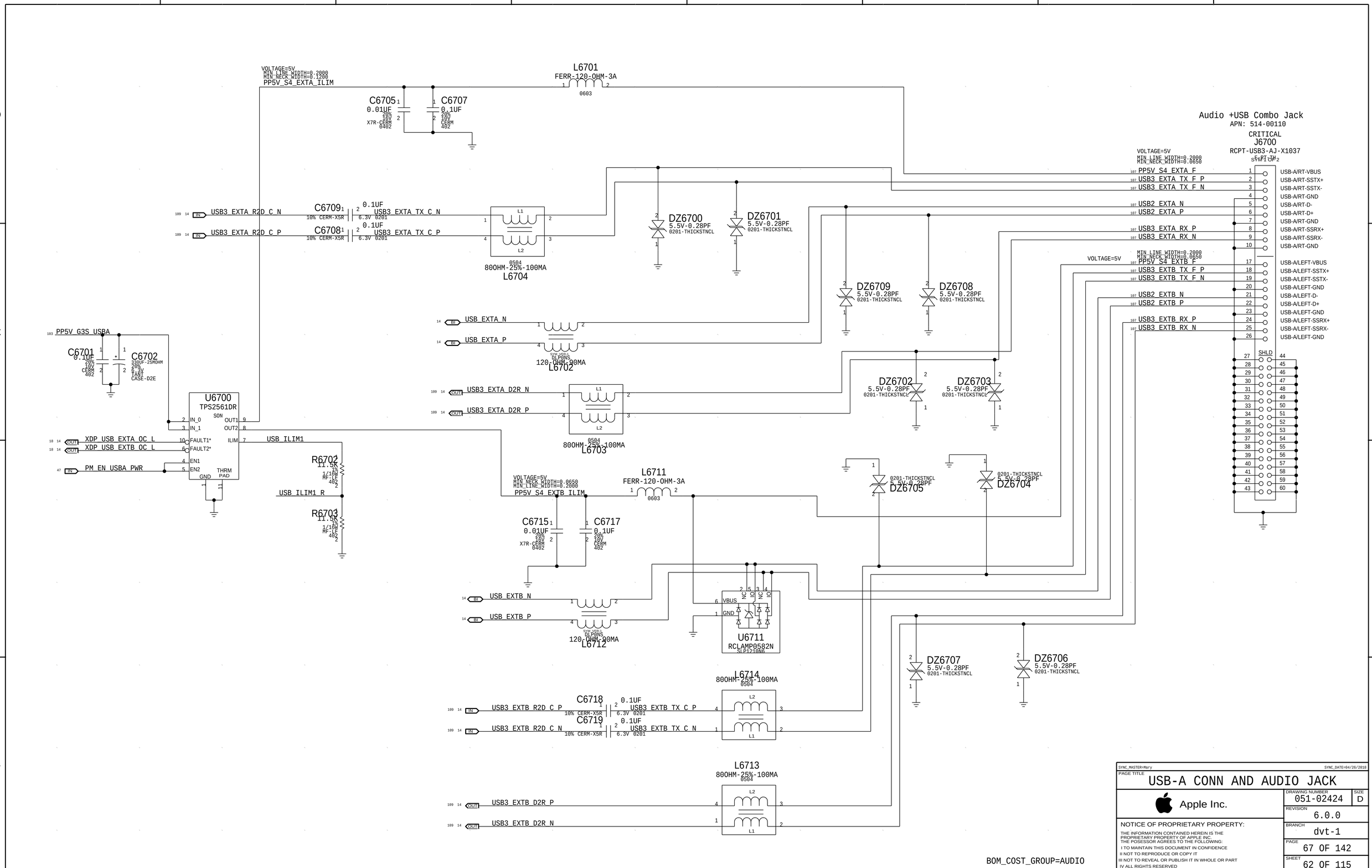
VOLTAGE=5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
PP5V_S4_EXTA_ILIM
L6701
FERR-120-OHM-3A
0603
C6705
0.01UF
20%
16V
X7R-CERM
0402
C6707
0.1UF
20%
16V
CERM
402
Audio +USB Combo Jack
APN: 514-00110
CRITICAL
J6700
RCPT-USB3-AJ-X1037
USB3_EXTA_R2D_C_N
USB3_EXTA_R2D_C_P
C6709
C6708
0.1UF
10% CERM-X5R
6.3V 0201
USB3_EXTA_TX_C_N
USB3_EXTA_TX_C_P
L6704
80OHM-25%-100MA
DZ6700
DZ6701
5.5V-0.28PF
0201-THICKSTNCL
PP5V_S4_EXTA_F
USB3_EXTA_TX_F_P
USB3_EXTA_TX_F_N
USB2_EXTA_N
USB2_EXTA_P
USB3_EXTA_RX_P
USB3_EXTA_RX_N
USB-A/RT-VBUS
USB-A/RT-SSTX+
USB-A/RT-SSTX-
USB-A/RT-GND
USB-A/RT-D-
USB-A/RT-D+
USB-A/RT-GND
USB-A/RT-SSRX+
USB-A/RT-SSRX-
USB-A/RT-GND
VOLTAGE=5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0850
PP5V_S4_EXTB_F
USB3_EXTB_TX_F_P
USB3_EXTB_TX_F_N
USB2_EXTB_N
USB2_EXTB_P
USB3_EXTB_RX_P
USB3_EXTB_RX_N
USB-A/LEFT-VBUS
USB-A/LEFT-SSTX+
USB-A/LEFT-SSTX-
USB-A/LEFT-GND
USB-A/LEFT-D-
USB-A/LEFT-D+
USB-A/LEFT-GND
USB-A/LEFT-SSRX+
USB-A/LEFT-SSRX-
USB-A/LEFT-GND
SHLD
DZ6709
DZ6708
DZ6702
DZ6703
DZ6705
DZ6704
DZ6707
DZ6706
PP5V_G3S_USBA
C6701
0.1UF
20%
16V
CERM
402
C6702
330UF-25MOHM
20%
6.3V
TANT
CASE-D2E
U6700
TPS2561DR
SON
IN_0
IN_1
OUT1
OUT2
FAULT1*
FAULT2*
ILIM
EN1
EN2
GND
THRM PAD
XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L
PM_EN_USBA_PWR
USB_ILIM1
R6702
11.5K
1/16W
MF-LF
402
USB_ILIM1_R
R6703
11.5K
1/16W
MF-LF
402
USB_EXTA_N
USB_EXTA_P
L6702
120-OHM-90MA
DLP0NS
USB3_EXTA_D2R_N
USB3_EXTA_D2R_P
L6703
80OHM-25%-100MA
VOLTAGE=5V
MIN_NECK_WIDTH=0.0850
MIN_LINE_WIDTH=0.2000
PP5V_S4_EXTB_ILIM
L6711
FERR-120-OHM-3A
C6715
0.01UF
20%
16V
X7R-CERM
0402
C6717
0.1UF
20%
16V
CERM
402
USB_EXTB_N
USB_EXTB_P
L6712
120-OHM-90MA
DLP0NS
U6711
RCLAMP0582N
SLP1210N6
VBUS
GND
L6714
80OHM-25%-100MA
0504
C6718
C6719
USB3_EXTB_R2D_C_P
USB3_EXTB_R2D_C_N
USB3_EXTB_TX_C_P
USB3_EXTB_TX_C_N
L6713
80OHM-25%-100MA
0504
USB3_EXTB_D2R_P
USB3_EXTB_D2R_N
BOM_COST_GROUP=AUDIO
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
USB-A CONN AND AUDIO JACK
Apple Inc.
DRAWING NUMBER
051-02424
SIZE
D
REVISION
6.0.0
BRANCH
dvt-1
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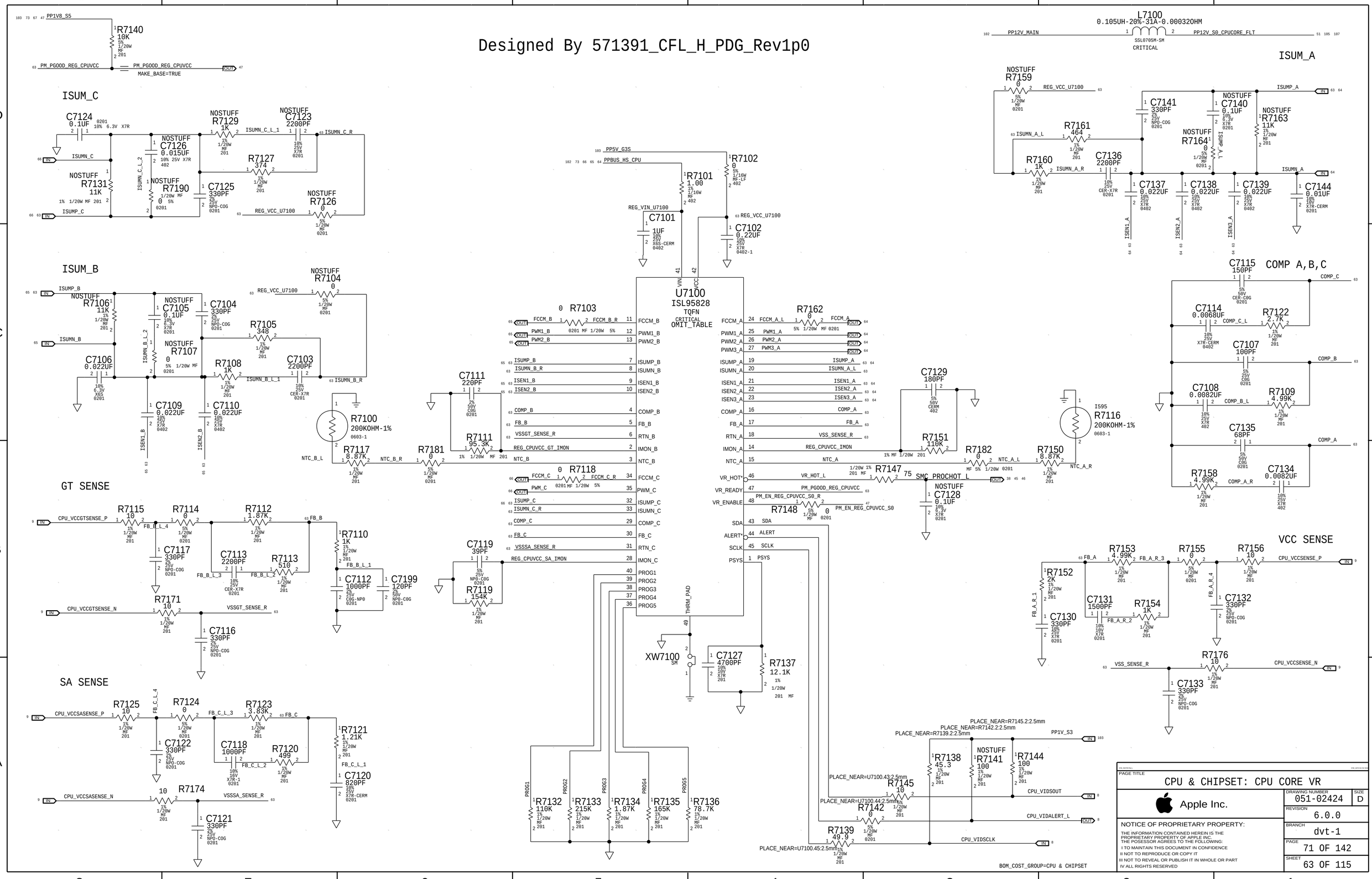
Designed By 571391_CFL_H_PDG_Rev1p0
ISUM_C
ISUM_B
GT SENSE
SA SENSE
ISUM_A
COMP A,B,C
VCC SENSE
U7100
ISL95828
TQFN
CRITICAL
OMIT_TABLE
L7100
0.105UH-20%-31A-0.000320HM
SSL0705M-SM
CRITICAL
PP1V8_S5
PM_PGOOD_REG_CPUVCC
MAKE_BASE=TRUE
PP12V_MAIN
PP12V_S0_CPUCORE_FLT
PP5V_G3S
PPBUS_HS_CPU
REG_VCC_U7100
REG_VIN_U7100
CPU_VCCGTSENSE_P
CPU_VCCGTSENSE_N
VSSGT_SENSE_R
CPU_VCCSASENSE_P
CPU_VCCSASENSE_N
VSSSA_SENSE_R
VSS_SENSE_R
CPU_VCCSENSE_P
CPU_VCCSENSE_N
PP1V_S3
CPU_VIDSOUT
CPU_VIDALERT_L
CPU_VIDSCLK
SMC_PROCHOT_L
PLACE_NEAR=R7145.2:2.5mm
PLACE_NEAR=R7142.2:2.5mm
PLACE_NEAR=R7139.2:2.5mm
PLACE_NEAR=U7100.43:2.5mm
PLACE_NEAR=U7100.44:2.5mm
PLACE_NEAR=U7100.45:2.5mm
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
CPU & CHIPSET: CPU CORE VR
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CPU VCC Regulator

EDC = 128A
TDC = 91A
Fsw = 583KHz

CPU VCORE Phase 1

CPU VCORE Phase 2

CPU Phase 3

U7210 SIC621CD MLP-COMBO CRITICAL

U7230 SIC621CD MLP-COMBO CRITICAL

U7250 SIC621CD MLP-COMBO CRITICAL

PPBUS_HS_CPU

PP5V_G3S

PP5V_S0_VRD_VCIN_A1

PP5V_S0_VRD_VCIN_A2

PP5V_S0_VRD_VCIN_A3

BOOST_A_1_RC

BOOST_A_2_RC

BOOST_A_3_RC

BOOST_A_1

PHASE_A_1

BOOST_A_2

PHASE_A_2

BOOST_A_3

PHASE_A_3

SW_A_1

SW_A_2

SW_A_3

FCCM_A

PWM1_A

PWM2_A

PWM3_A

PPCPUVCC_S0_SENSE_1_1

PPCPUVCC_S0_SENSE_2_1

PPCPUVCC_S0_SENSE_3_1

PPVCC_S0_CPU_REG

REG_SNUBBER_CPUVCC_1

REG_SNUBBER_CPUVCC_2

REG_SNUBBER_CPUVCC_3

REG_CPUVCC_ISNS_1_P

REG_CPUVCC_ISNS_1_N

REG_CPUVCC_ISNS_2_P

REG_CPUVCC_ISNS_2_N

REG_CPUVCC_ISNS_3_P

REG_CPUVCC_ISNS_3_N

ISEN1_A

ISEN2_A

ISEN3_A

ISUMN_A

ISUMP_A

L7210 0.22UH-20%-65A-0.000640HM PIME104T-SM

L7230 0.22UH-20%-65A-0.000640HM PIME104T-SM

L7250 0.22UH-20%-65A-0.000640HM PIME104T-SM

R7210 0.0005 1% 1W MF 0612-2

R7230 0.0005 1% 1W MF 0612-2

R7250 0.0005 1% 1W MF 0612-2

R7219 1K 1% 1/20W MF 201

R7220 100K 1% 1/20W MF 201

R7239 1K 1% 1/20W MF 201

R7240 100K 1% 1/20W MF 201

R7259 1K 1% 1/20W MF 201

R7260 100K 1% 1/20W MF 201

NO_XNET_CONNECTION=1

BOM_COST_GROUP=CPU & CHIPSET

DRAWING LAST_MODIFIED=Thu Jul 12 17:56:51 2018

PAGE TITLE: CPU & CHIPSET: CPU CORE VR (VCC)

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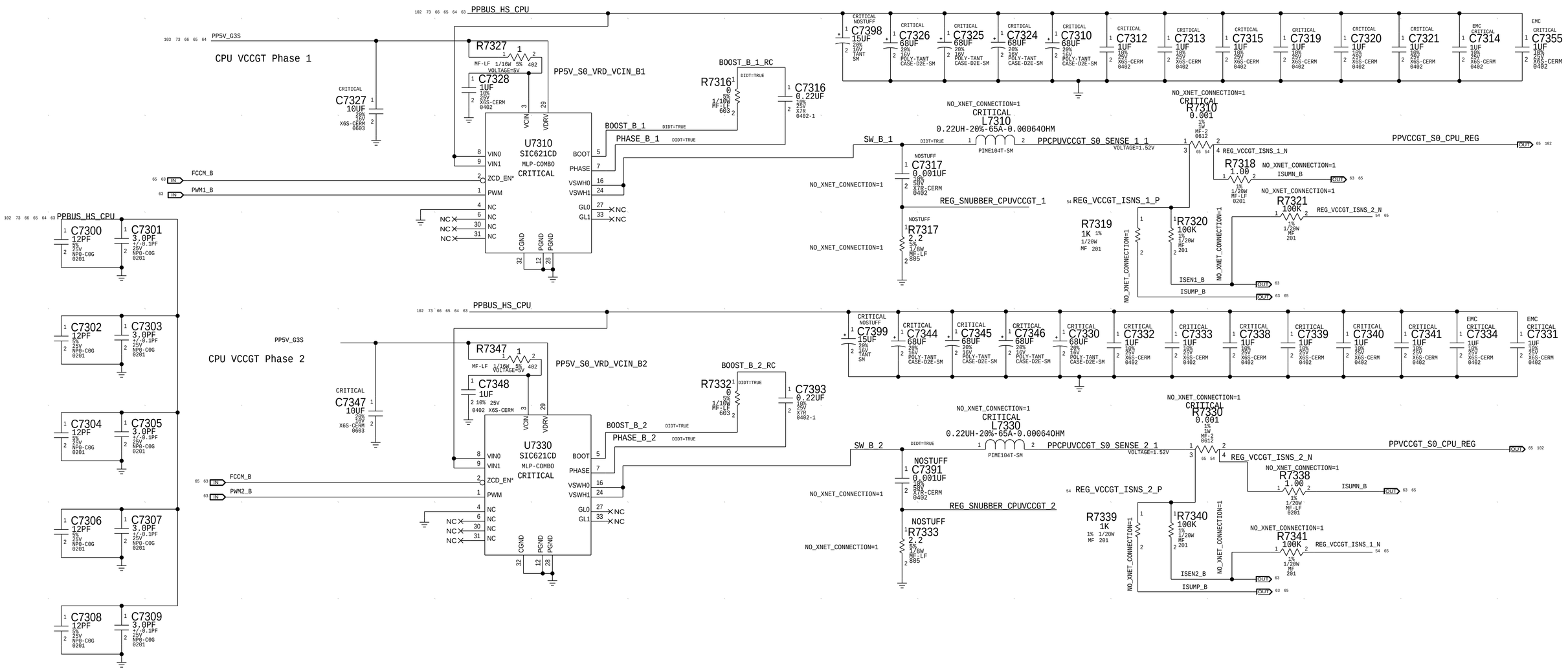
CPU VCCGT Regulator

EDC = 32A

TDC = 25A

Fsw = 583KHz



DRAWING	LAST_MODIFIED=Thu Jul 12 17:57:07 2018
PAGE TITLE	CPU & CHIPSET: CPU CORE VR (VCCGT)
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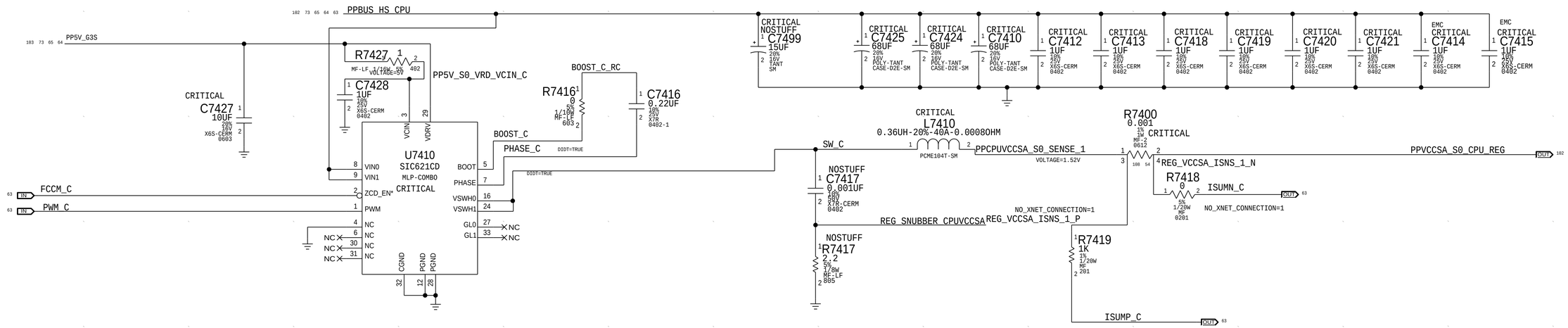
BOM_COST_GROUP=CPU & CHIPSET

CPU VCCSA Regulator

EDC = 11.1A

TDC = 10A

Fsw = 583KHz



BOM_COST_GROUP=CPU & CHIPSET

DRAWING	LAST_MODIFIED=Thu Jul 12 17:57:07 2018
PAGE TITLE	CPU & CHIPSET: CPU CORE VR (VCCSA)
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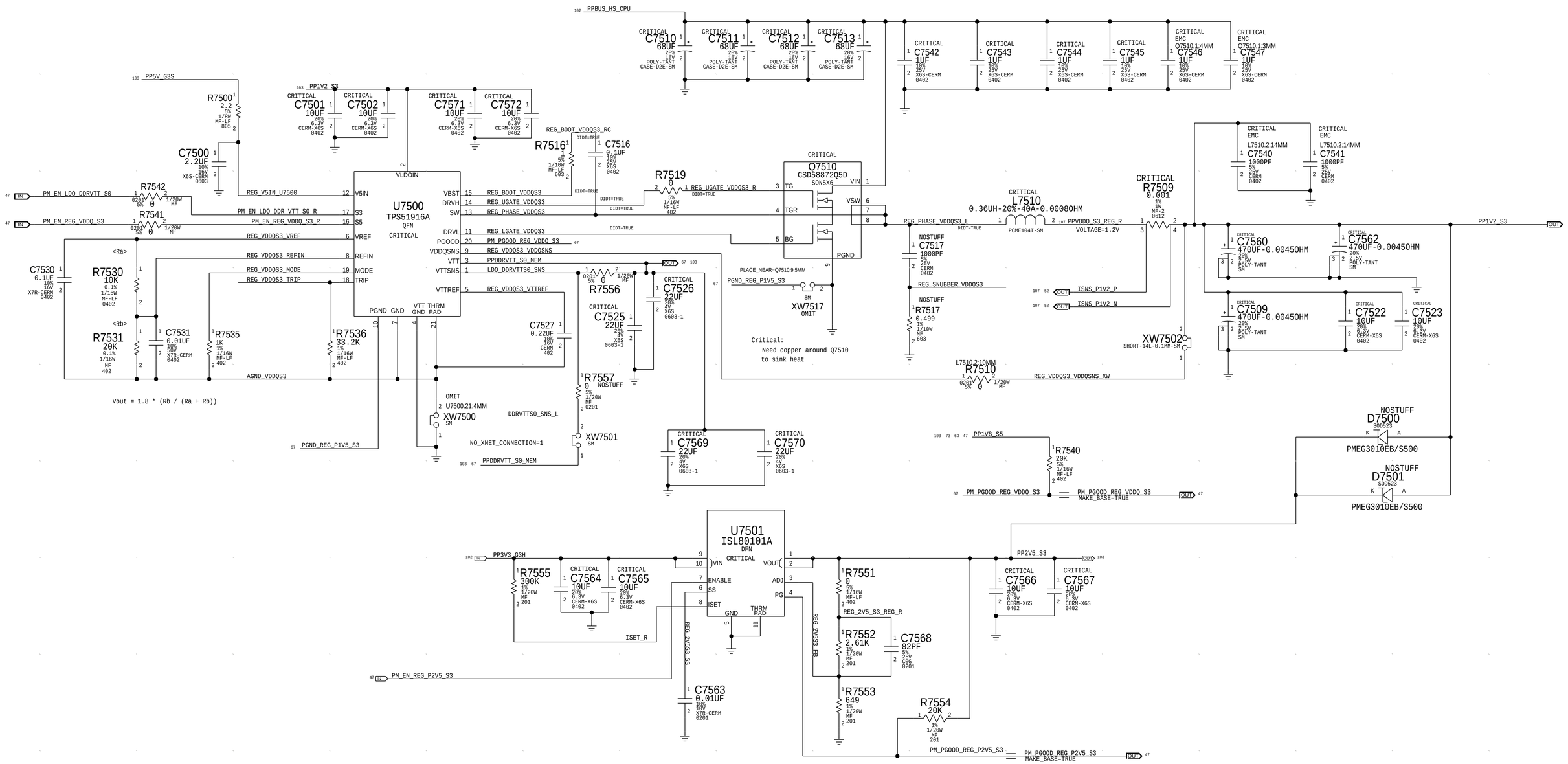
VDDQ S3 REGULATOR

VDDQ = 1.2V @ 8.43A (EDC)

VTT = 0.6V @ 1A (EDC)

VPP = 2.5V @ 0.384A (EDC)

Fsw = 500KHz



PAGE TITLE
CPU & CHIPSET: CPU VDDQ VR

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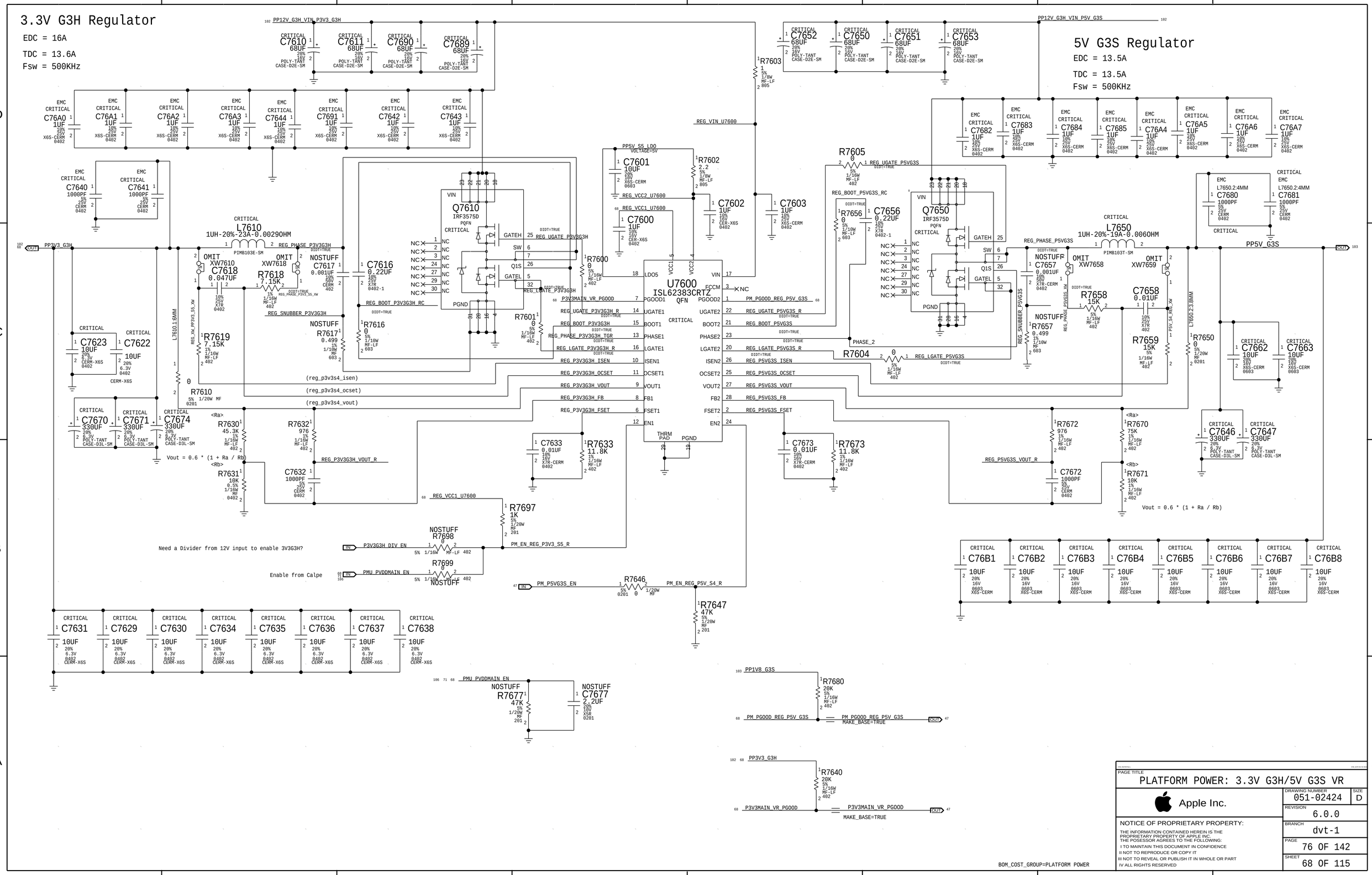
3.3V G3H Regulator
EDC = 16A
TDC = 13.6A
Fsw = 500KHz
5V G3S Regulator
EDC = 13.5A
TDC = 13.5A
Fsw = 500KHz
PP12V_G3H_VIN_P3V3_G3H
PP12V_G3H_VIN_P5V_G3S
PP3V3_G3H
PP5V_G3S
L7610 1UH-20%-23A-0.0029OHM
L7650 1UH-20%-19A-0.0060HM
Q7610 IRF3575D
Q7650 IRF3575D
U7600 ISL62383CRTZ QFN
Vout = 0.6 * (1 + Ra / Rb)
Need a Divider from 12V input to enable 3V3G3H?
Enable from Calpe
PAGE TITLE
PLATFORM POWER: 3.3V G3H/5V G3S VR
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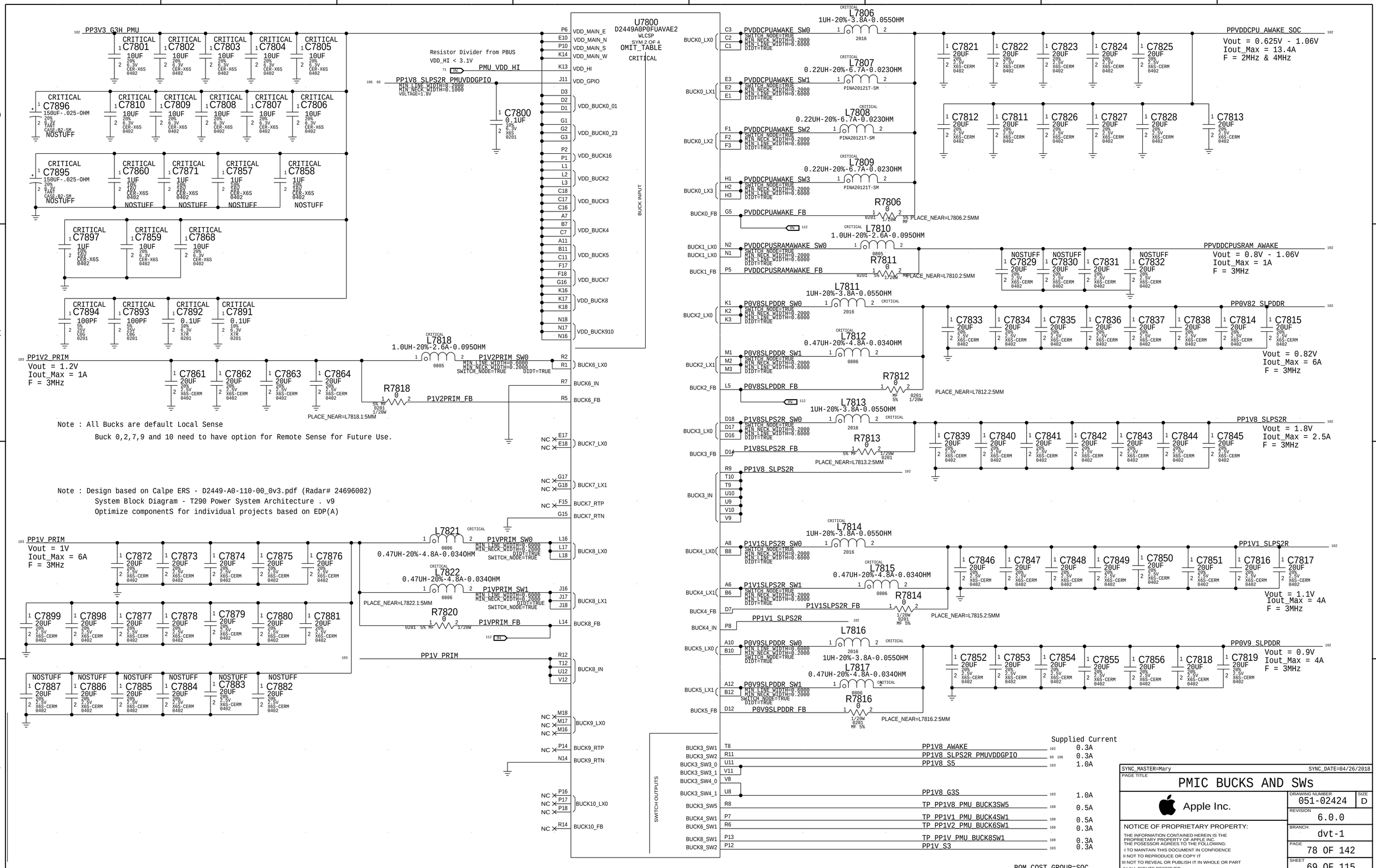
U7800
D2449A0P0FUAVAE2
WLCSP
SYM 2 OF 4
OMIT_TABLE
CRITICAL
BUCK INPUT
PP3V3_G3H_PMU
Resistor Divider from PBUS
VDD_HI < 3.1V
PMU_VDD_HI
PP1V8_SLPS2R_PMUVDDGPIO
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.8V
VDD_MAIN_E
VDD_MAIN_N
VDD_MAIN_S
VDD_MAIN_W
VDD_HI
VDD_GPIO
VDD_BUCK0_01
VDD_BUCK0_23
VDD_BUCK16
VDD_BUCK2
VDD_BUCK3
VDD_BUCK4
VDD_BUCK5
VDD_BUCK7
VDD_BUCK8
VDD_BUCK910
PP1V2_PRIM
Vout = 1.2V
Iout_Max = 1A
F = 3MHz
L7818
1.0UH-20%-2.6A-0.0950HM
P1V2PRIM_SW0
P1V2PRIM_FB
R7818
PLACE_NEAR=L7818.1:5MM
BUCK6_LX0
BUCK6_IN
BUCK6_FB
BUCK7_LX0
BUCK7_LX1
BUCK7_RTP
BUCK7_RTN
Note : All Bucks are default Local Sense
Buck 0,2,7,9 and 10 need to have option for Remote Sense for Future Use.
Note : Design based on Calpe ERS - D2449-A0-110-00_0v3.pdf (Radar# 24696002)
System Block Diagram - T290 Power System Architecture . v9
Optimize componentS for individual projects based on EDP(A)
PP1V_PRIM
Vout = 1V
Iout_Max = 6A
F = 3MHz
L7821
0.47UH-20%-4.8A-0.0340HM
P1VPRIM_SW0
L7822
0.47UH-20%-4.8A-0.0340HM
P1VPRIM_SW1
PLACE_NEAR=L7822.1:5MM
R7820
P1VPRIM_FB
BUCK8_LX0
BUCK8_LX1
BUCK8_FB
BUCK8_IN
BUCK9_LX0
BUCK9_RTP
BUCK9_RTN
BUCK10_LX0
BUCK10_FB
PP0V8_SLPDDR
Vout = 0.82V
Iout_Max = 6A
F = 3MHz
PP1V8_SLPS2R
Vout = 1.8V
Iout_Max = 2.5A
F = 3MHz
PP1V1_SLPS2R
Vout = 1.1V
Iout_Max = 4A
F = 3MHz
PP0V9_SLPDDR
Vout = 0.9V
Iout_Max = 4A
F = 3MHz
SWITCH OUTPUTS
Supplied Current
PP1V8_AWAKE 0.3A
PP1V8_SLPS2R_PMUVDDGPIO 0.3A
PP1V8_S5 1.0A
PP1V8_G3S 1.0A
TP_PP1V8_PMU_BUCK3SW5 0.5A
TP_PP1V1_PMU_BUCK4SW1 0.5A
TP_PP1V2_PMU_BUCK6SW1 0.3A
TP_PP1V_PMU_BUCK8SW1 0.3A
PP1V_S3 0.3A
BOM_COST_GROUP=SOC
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
PMIC BUCKS AND SWs
Apple Inc.
DRAWING NUMBER
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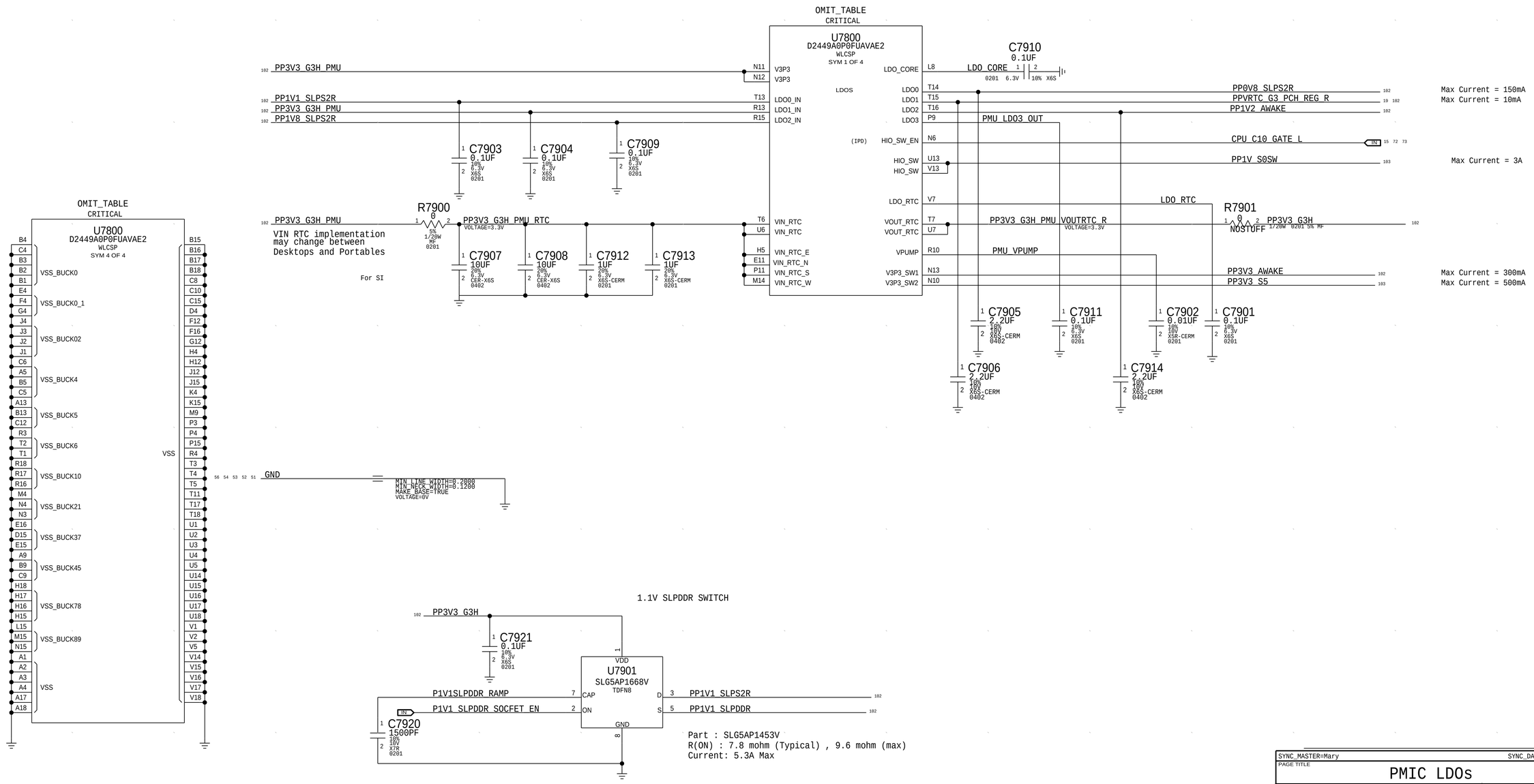

BOM_COST_GROUP=SOC

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
PMIC LDOs

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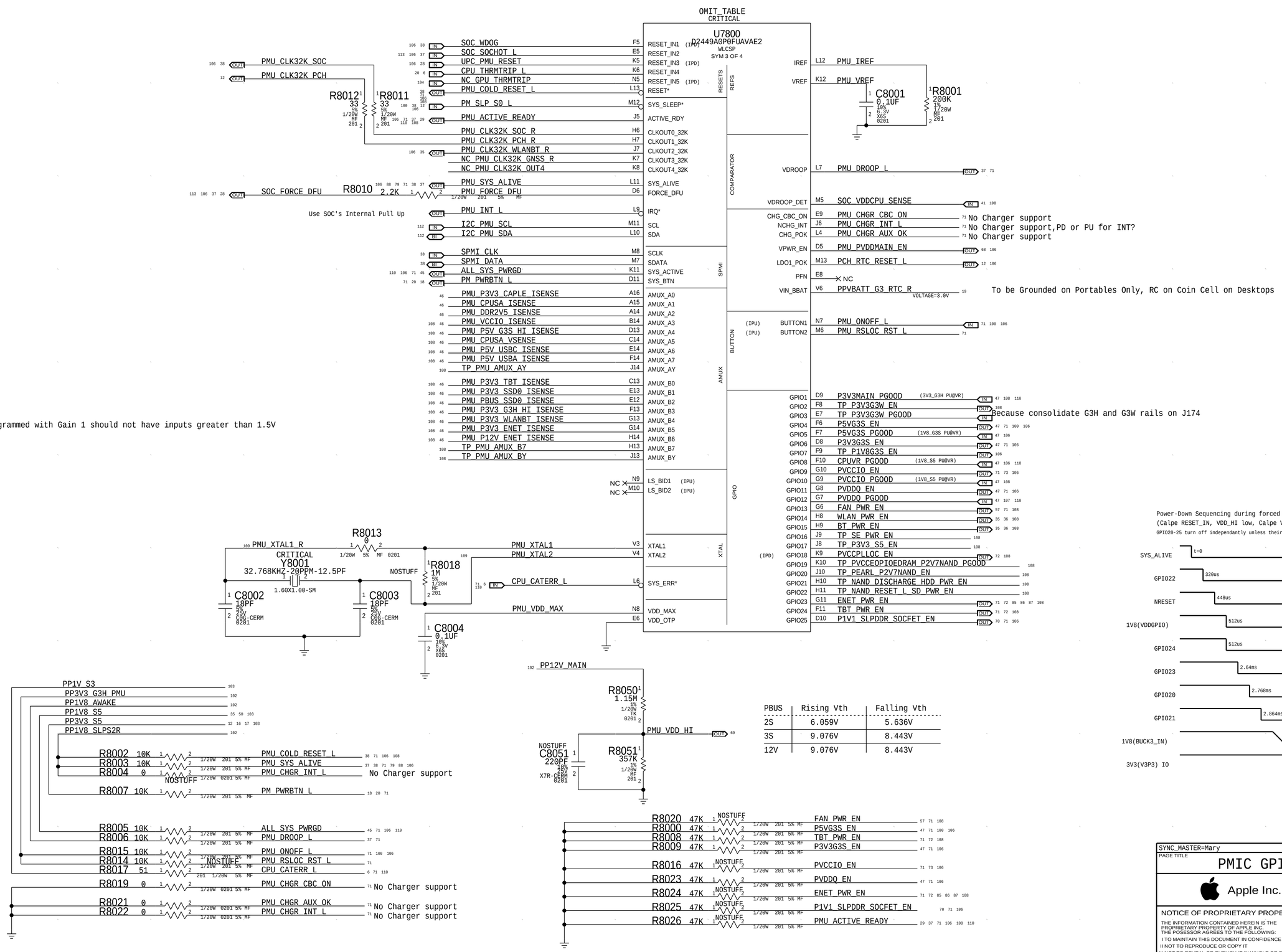


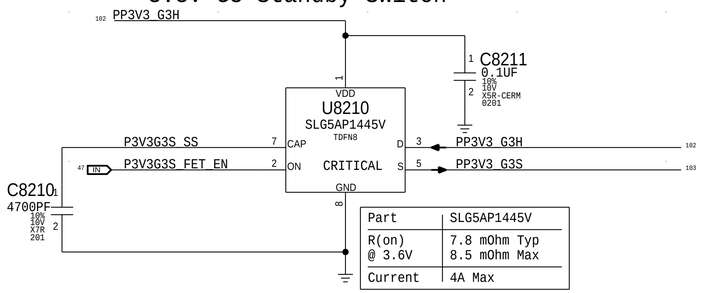
PBUS	Rising Vth	Falling Vth
2S	6.059V	5.636V
3S	9.076V	8.443V
12V	9.076V	8.443V

System Power States

	System State:	Shutdown (G3H)		Standby (G3S)		Standby (S4)		Sleep (S0i/S3)		Run (S0)
	CPU/PCH State:	Off (RTC Only)		Off (RTC Only)		Standby		Sleep		Run
Rails	SoC State:	S2R	Awake	S2R	Awake	S2R	Awake	S2R	Awake	Awake
PP*_S2R (0.8,1.1,1.8V)		On	On	On	On	On	On	On	On	On
PP*_DDR (0.8,0.9,1.1V)		Off	On	Off	On	Off	On	Off	On	On
PP*_AWAKE (CPU,SRAM,1.2,1.8,3.3V)		Off	On	Off	On	Off	On	Off	On	On
PP3V3_G3H (VR1)		On	On	On	On	On	On	On	On	On
PP1S_G3H		On	On	On	On	On	On	On	On	On
PP3V3_G3W		Off	On	Off	On	On	On	On	On	On
PP*_G3S (1.8,3.3,5V)		Off	On	On	On	On	On	On	On	On
PP*_S5 (1.8,3.3V)		Off	Off	Off	Off	On	On	On	On	On
CPU/PCH VRs		Off	Off	Off	Off	Off/On	Off/On	Off/On	Off/On	On

* System: Shutdown Awake is a transition state only.
* SoC: SLP_DDR is a transition state only.
* CPU/PCH: S4 is only used by desktops for USB wakes.
* CPU/PCH: S5 is a transition state. May also be used for RTC wakes.

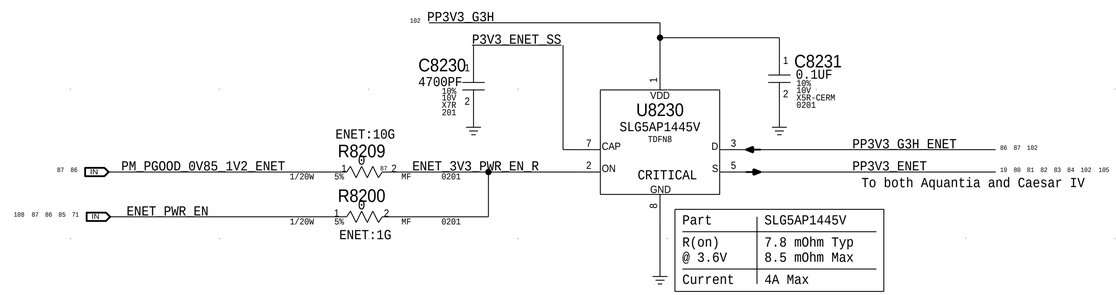
3.3V G3 Standby Switch



Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

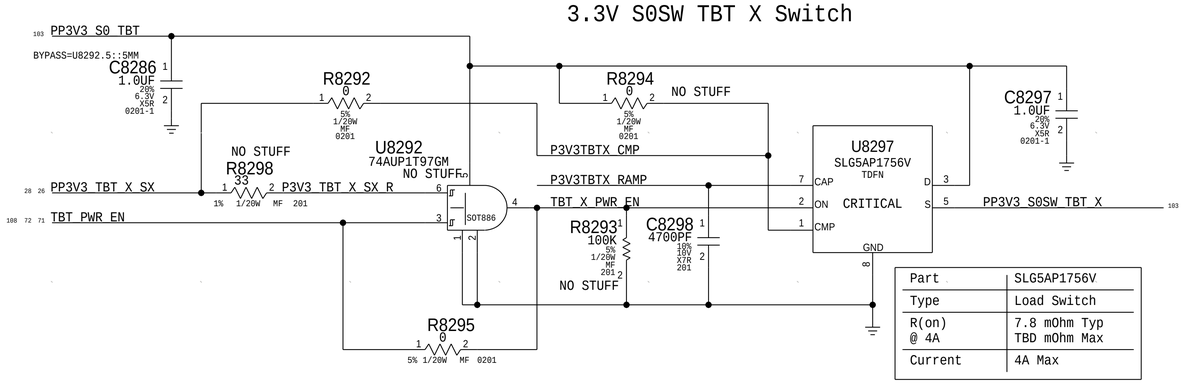
Based off rdar://30356539. 3V3_G3W can be combined into 3V3_G3H,

3.3V ENET Switch



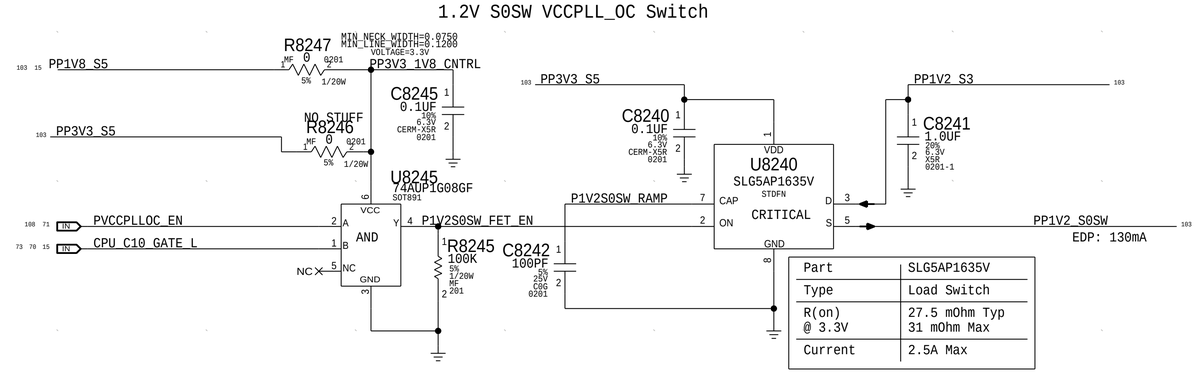
Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

3.3V S0SW TBT X Switch



Part	SLG5AP1756V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

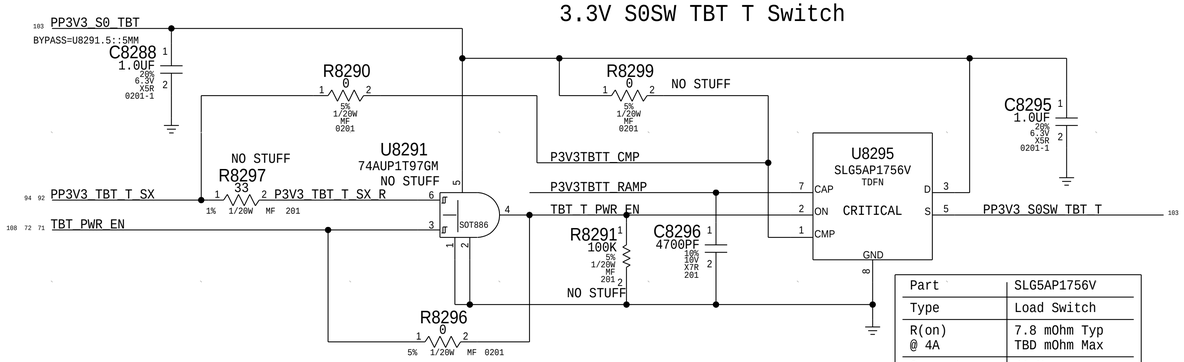
1.2V S0SW VCCPLL_OC Switch



Part	SLG5AP1635V
Type	Load Switch
R(on) @ 3.3V	27.5 mOhm Typ 31 mOhm Max
Current	2.5A Max

VCCPLL_OC has turn-on requirement of
11uS min and 240uS max
from EN to 1.1V

3.3V S0SW TBT T Switch



Part	SLG5AP1756V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
Power FETs

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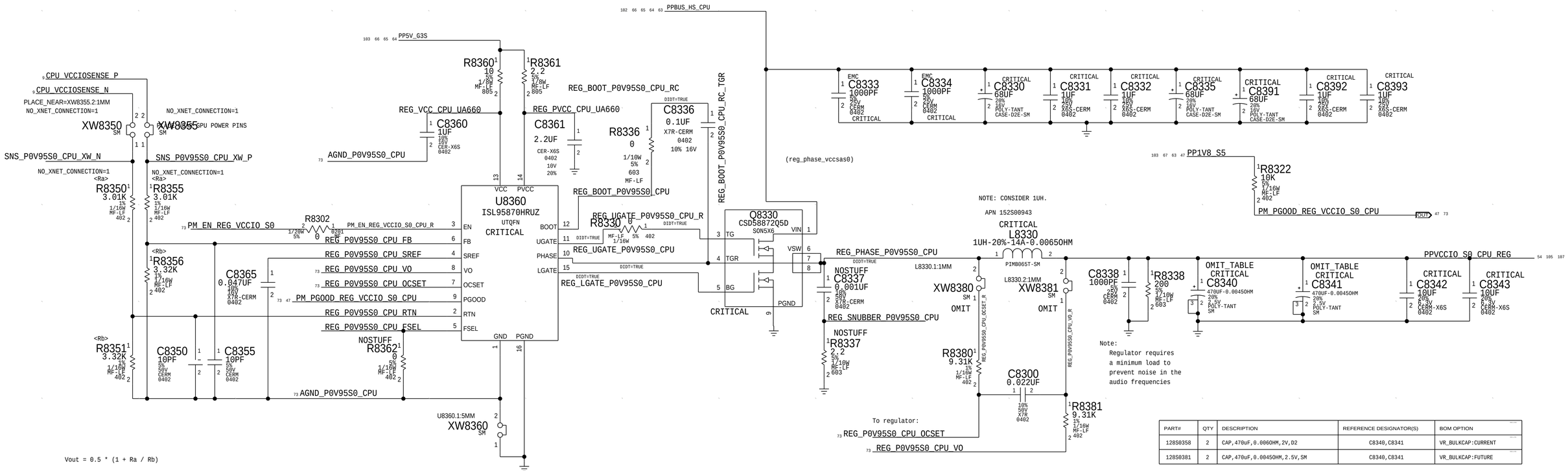
VCCIO S0 REGULATOR

EDC = 6.4A

TDC = 6.4A

Fsw = 500KHz



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0358	2	CAP,470uF,0.0060HM,2V,D2	C8340,C8341	VR_BULKCAP:CURRENT
128S0381	2	CAP,470uF,0.00450HM,2.5V,SM	C8340,C8341	VR_BULKCAP:FUTURE

BOM_COST_GROUP=CPU & CHIPSET

DRAWING LAST_MODIFIED=Thu Jul 12 17:57:13 2018

PAGE TITLE: CPU & CHIPSET: CPU VCCIO VR

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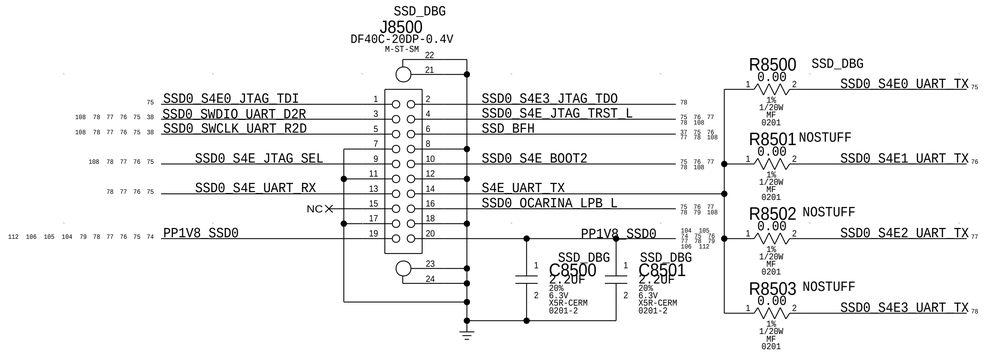

BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

SSD DEBUG AND SUPPORT

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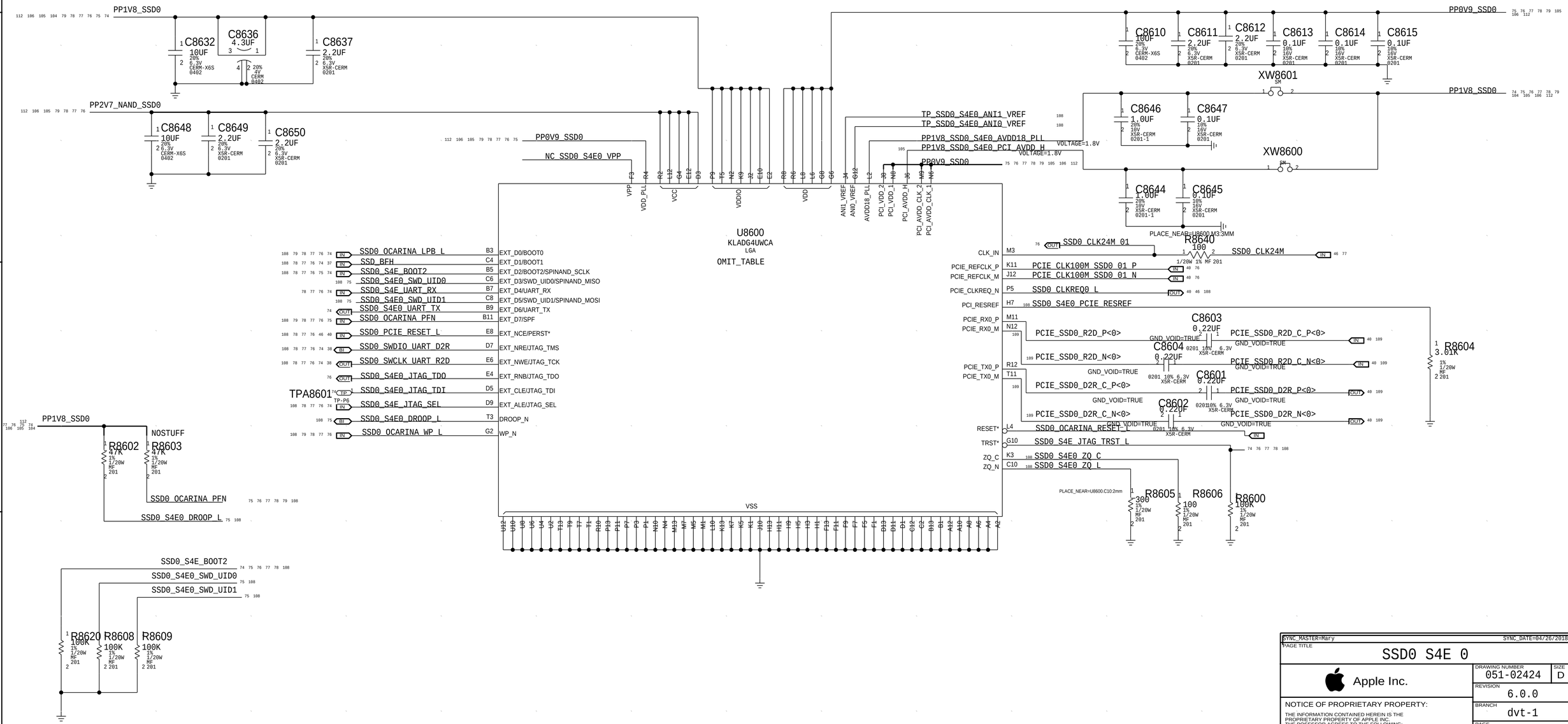

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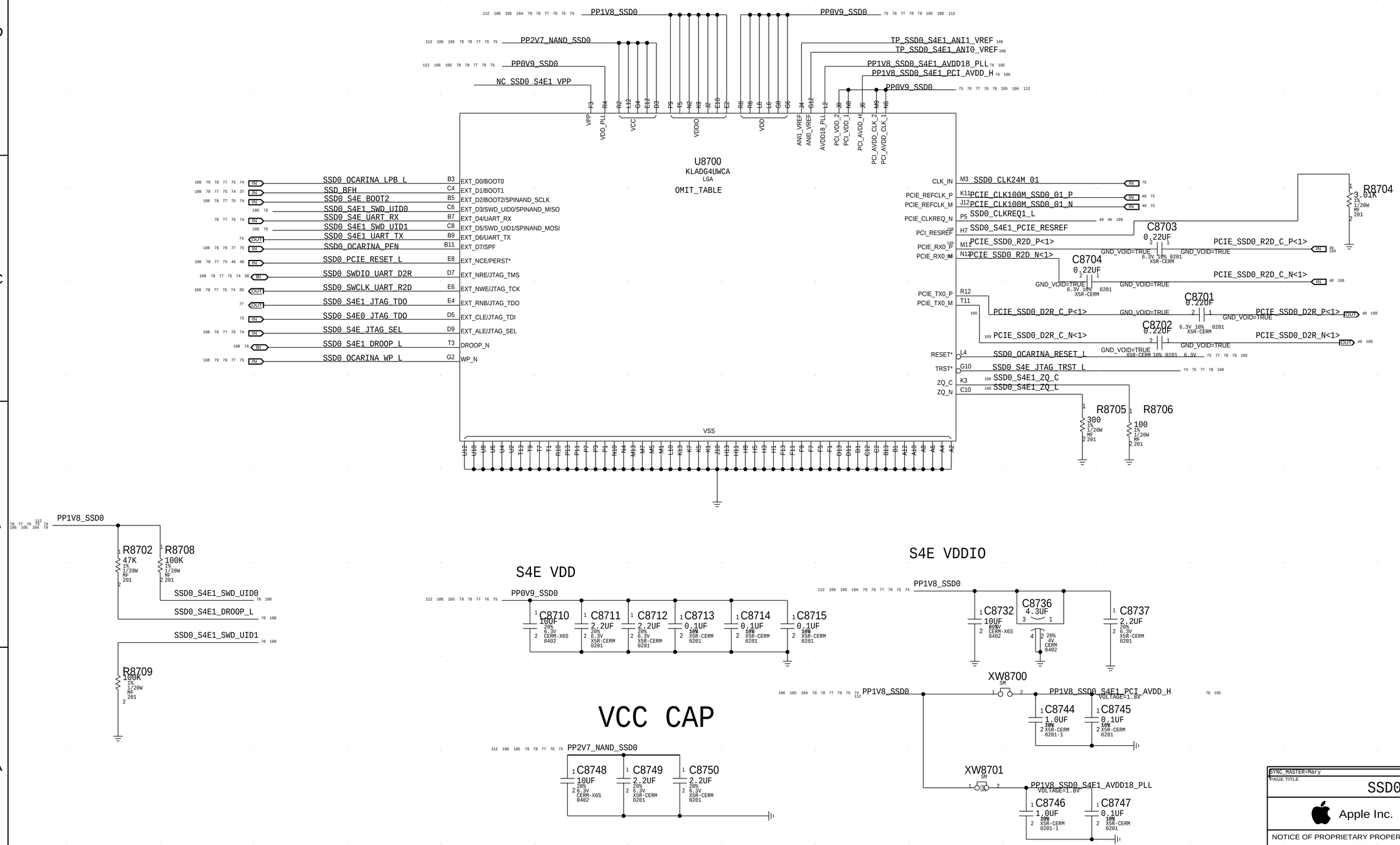
S4E1



BOM_COST_GROUP=SSD

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

SSD0 S4E 1

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

BRANCH dvt-1

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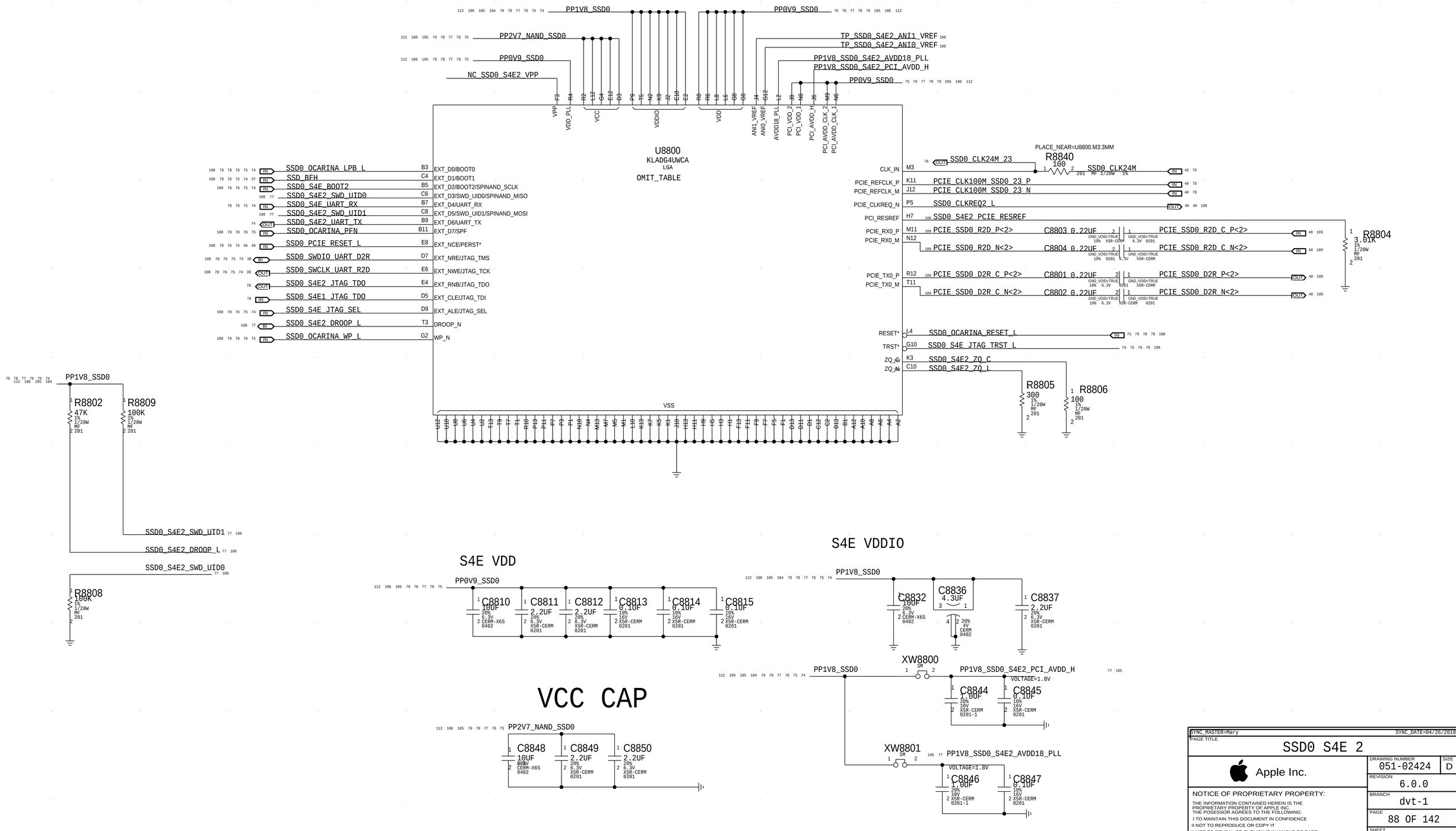

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SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SSD0 S4E 2

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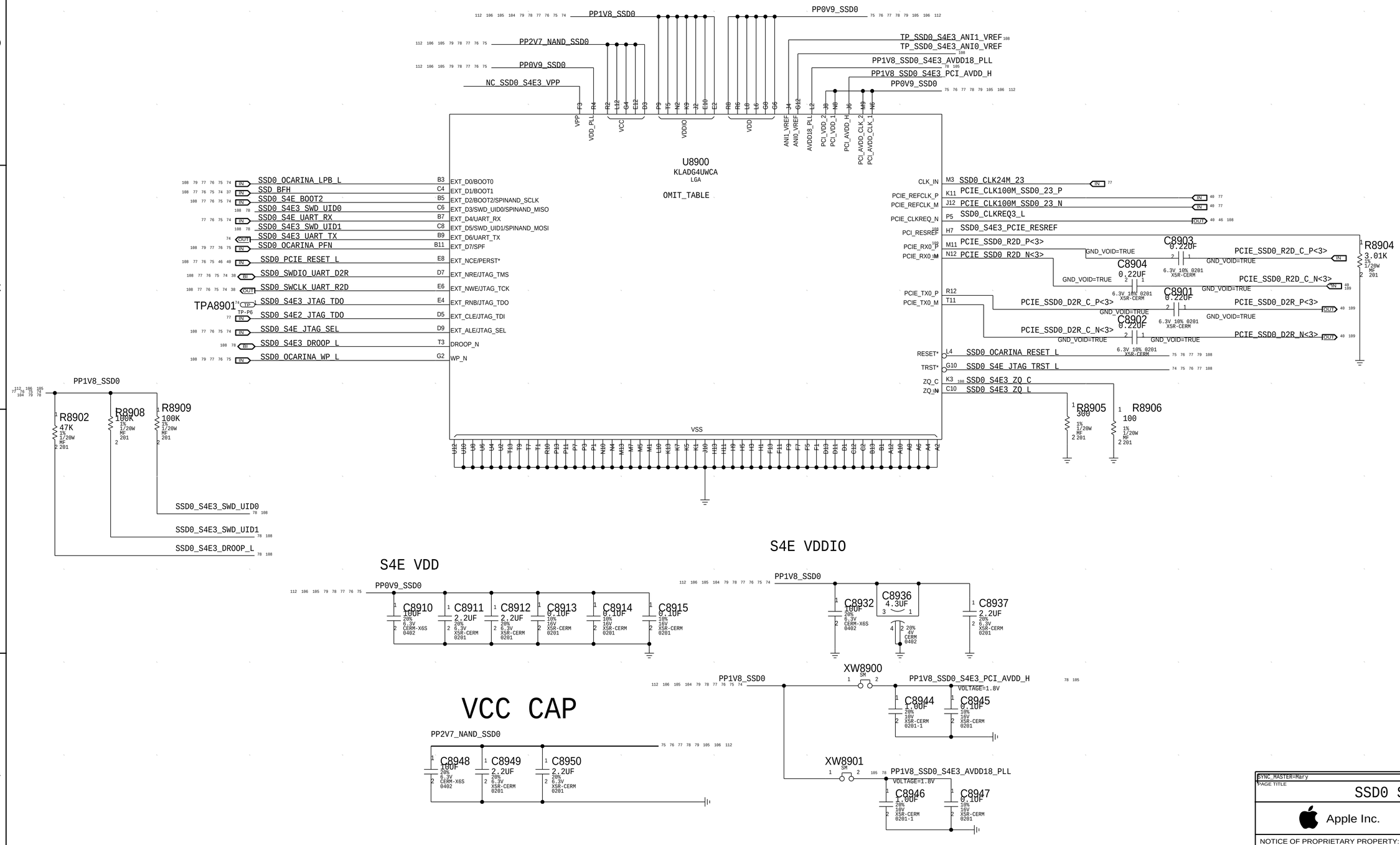
S4E3



BOM_COST_GROUP=SSD

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: SSD0 S4E 3

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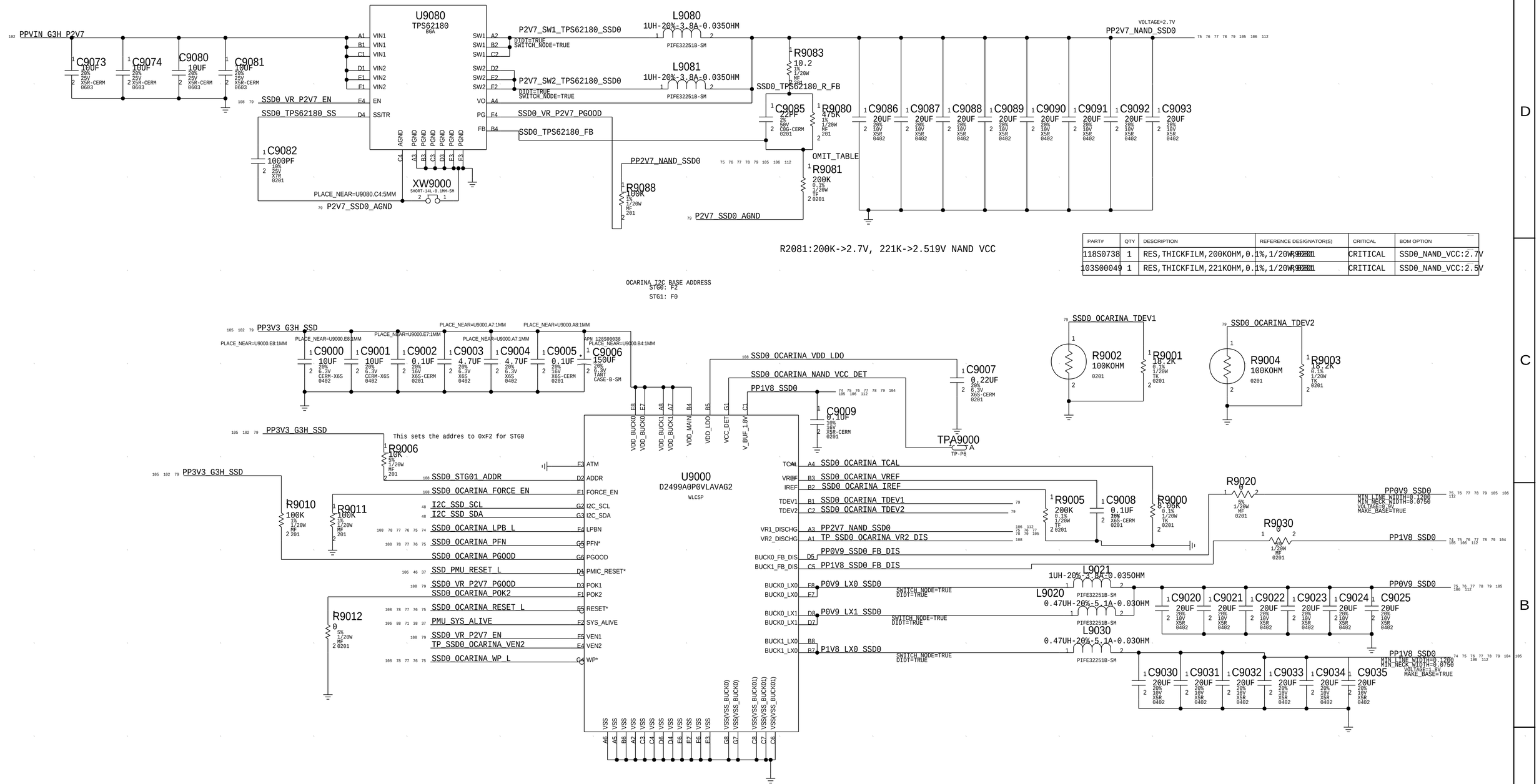

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0738	1	RES,THICKFILM,200KOHM,0.1%,1/20W,0201	R9081	CRITICAL	SSD0_NAND_VCC:2.7V
103S00049	1	RES,THICKFILM,221KOHM,0.1%,1/20W,0201	R9081	CRITICAL	SSD0_NAND_VCC:2.5V

BOM_COST_GROUP=SSD

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

SSD0 PMIC & VR

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

ENET:1G CRITICAL L9300 FERR-600-OHM-300MA-0.850OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C9300 0.1UF 10% 16V X5R-CERM 0201 ENET:1G

VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT
ENET_XTALVDDH
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

ENET:1G CRITICAL L9305 FERR-600-OHM-300MA-0.850OHM 0402
PP3V3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C9305 0.1UF 10% 16V X5R-CERM 0201 ENET:1G

ENET:1G CRITICAL L9310 FERR-600-OHM-300MA-0.850OHM 0402
PP3V3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
R9310 4.7K 5% 1/16W MF-LF 402 ENET:1G
C9310 0.1UF 10% 16V X5R-CERM 0201 ENET:1G
C9311 0.1UF 10% 16V X5R-CERM 0201 ENET:1G

ENET:1G R9340 4.7K 5% 1/16W MF-LF 402
ENET:1G R9341 4.7K 5% 1/16W MF-LF 402
ENET:1G C9315 4.7UF 20% 6.3V X5R-CERM 402
ENET:1G C9316 0.1UF 10% 16V X5R-CERM 0201

PM_SLP_S3_L
ENET:1G R9342 1K 5% 1/16W MF-LF 402
Current Limiting Resistor

ENET_SR_LX
PP1V2_ENET_INTREG
Internal 1.2V Switching Regulator pins.

PP1V2_ENET_INTREG
396mA (1000base-T, Caesar II)

ENET:1G CRITICAL L9320 FERR-600-OHM-300MA-0.850OHM 0402
PP1V2_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
C9321 0.1UF 10% 16V X5R-CERM 0201 ENET:1G
C9320 4.7UF 20% 6.3V X5R-CERM1 402 ENET:1G

ENET:1G CRITICAL L9325 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
C9326 0.1UF 10% 16V X5R-CERM 0201 ENET:1G
C9325 4.7UF 20% 6.3V X5R-CERM1 402 ENET:1G

ENET:1G CRITICAL L9330 FERR-600-OHM-300MA-0.850OHM 0402
PP1V2_ENET_PHY_GHYPLL
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=1.2V
C9331 0.1UF 10% 16V X5R-CERM 0201 ENET:1G
C9330 4.7UF 20% 6.3V X5R-CERM1 402 ENET:1G

C9336 0.1UF 10% 16V X5R-CERM 0201 ENET:1G
C9335 10UF 20% 6.3V X5R 603 ENET:1G

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

OMIT_TABLE
U9300
BCM57766A1KMLG
QFN-8X8
CAESAR IV

ENET_VMAIN_PRSNT — 58 VMAIN_PRSNT (IPD-ENET)
PCIE_ENET_1G_D2R_C_N — 27 PCIE_TXD_N
PCIE_ENET_1G_D2R_C_P — 28 PCIE_TXD_P
PCIE_ENET_1G_R2D_P — 33 PCIE_RXD_P
PCIE_ENET_1G_R2D_N — 34 PCIE_RXD_N
PCIE_CLK100M_ENET_1G_P — 31 PCIE_REFCLK_P
PCIE_CLK100M_ENET_1G_N — 30 PCIE_REFCLK_N
ENET_RESET_3V3_L — 11 PERST* (IPD)
ENET_CLKREQ_3V3_L — 12 CLKREQ* (OD)
PCIEDN_WAKE_ENET_L (See note) — 3 WAKE* (OD)
ENET_1G_LOW_PWR — 4 LOW_PWR (IPD)
SMB_ENET_SCL — 6 SMB_CLK
SMB_ENET_SDA — 10 SMB_DATA (IPD-ENETM)
ENET_1G_SCLK — 66 SCLK_SPD1000LED*
ENET_1G_MISO — 64 SI/EEDATA
ENET_1G_MOSI — 65 SO_LINKLED*
ENET_1G_CS_L — 63 CS*/EECLK
(IPU)
TP_ENET_1G_SERIAL_DO — 2 SPD100LED*/SERIAL_DO (OD)
ENET_TRAFFICLED_L — 67 TRAFFICLED*/SERIAL_DI (OD)
ENET_XTAL_IN — 18 XTALI
ENET_XTAL_OUT — 19 XTALO
ENET_RDAC — 38 RDAC
ENET:1G R9365 1.24K 1% 1/16W MF-LF 402

AVDDH 42, 48; BIASVDDH 37; XTALVDDH 17; VDDO 7, 20, 56, 62; SR_VDD 14; SR_VDDP 15; SR_LX 16; SR_VFB 13; AVDDL 39, 45, 51; PCIE_PLLVDDL 29, 32; GPHY_PLLVDDL 36; VDDC 35, 61

TRD0_P 40 — ENETCONN_MDI_P<0>
TRD0_N 41 — ENETCONN_MDI_N<0>
TRD1_P 44 — ENETCONN_MDI_P<1>
TRD1_N 43 — ENETCONN_MDI_N<1>
TRD2_P 46 — ENETCONN_MDI_P<2>
TRD2_N 47 — ENETCONN_MDI_N<2>
TRD3_P 50 — ENETCONN_MDI_P<3>
TRD3_N 49 — ENETCONN_MDI_N<3>

PP3V3R1V8_ENET_LR_OUT
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V MAKE_BASE=TRUE
ENET:1G C9380 4.7UF 20% 6.3V X5R-CERM1 402
ENET:1G C9381 0.1UF 10% 16V X5R-CERM 0201
ENET:1G C9382 0.1UF 10% 16V X5R-CERM 0201
PP3V3R1V8_ENET_LR_OUT

GPIO_0/CR_ACT_LED* 5 — NC
GPIO_1/LR_OUT 8
GPIO_2/MEDIA_SENSE 9 — ENET_1G_MEDIA_SENSE
(IPD)
NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.
SD_DETECT 1 (IPx-ENET) — NC
CR_CMD 26 (IPU-ENET) — NC
CR_CLK 21 — NC
CR_DATA0 25 — NC
CR_DATA1 24 — NC
CR_DATA2 23 — NC
CR_DATA3 22 — NC
CR_DATA4 52 — NC
CR_DATA5 53 — NC
CR_DATA6 54 — NC
CR_DATA7 55 — NC
(IPU-ENET)
MS_INS* 59 (IPU-ENET) — NC
CR_LED*/CR_BUS_PWR 60 (IPU-ENET) — NC
CR_WP* 57 (IPU-ENET) — NC
SR_DISABLE 68 (NO IPU OR IPD-ENET) — ENET_SR_DISABLE (See note)
THRM_PAD 69
ENET 1.2V SR IS ENABLED IF FLOATING.

CONTROL SIGNAL TO LIGHT LED OR CONTROL SD BUS POWER.

R9381 1K 5% 1/16W MF-LF 402 ENET:1G
ENET supports both active-levels for WP.

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin should have a 1K pull-down to GND

PCIEDN_WAKE_ENET_L (See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L TO PCIEDN_WAKE_L.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

PP3V3_ENET
ENET:1G C9390 0.1UF 10% 16V X5R-CERM 0201
U9390 AT45DB011D SOIC-8S1 OMIT_TABLE
VCC 6; GND 7
ENET_1G_SCLK — SCK 2
ENET_1G_CS_L — CS* 4
WP* 5
RESET* 3
SI 1 — ENET_1G_MOSI
SO 8 — ENET_1G_MISO
NOSTUFF R9390 4.7K 5% 1/16W MF-LF 402
ENET:1G R9397 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

ENET:1G C9340 15PF 2% 50V C0G-CERM 0402
ENET:1G C9341 15PF 2% 50V C0G-CERM 0402
ENET:1G CRITICAL Y9340 25.000MHZ-20PPM-12PF-85C 3.2X2.5MM-SM
NC NC
ENET_XTAL_OUT_R
ENET:1G R9343 0 5% 1/16W MF-LF 402
ENET_XTAL_OUT
NOSTUFF R9344 1M 5% 1/16W MF-LF 402
ENET_XTAL_IN
NOTE: 30 PPM crystal required

BOM_COST_GROUP=ETHERNET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018
PAGE TITLE: 1G ENET PHY (Caesar IV)
Apple Inc.
DRAWING NUMBER: 051-02424 SIZE: D
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BRANCH: dvt-1
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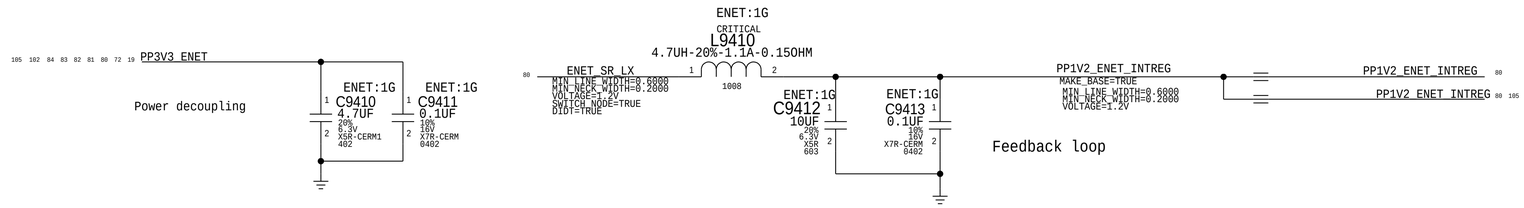
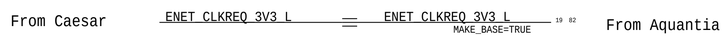
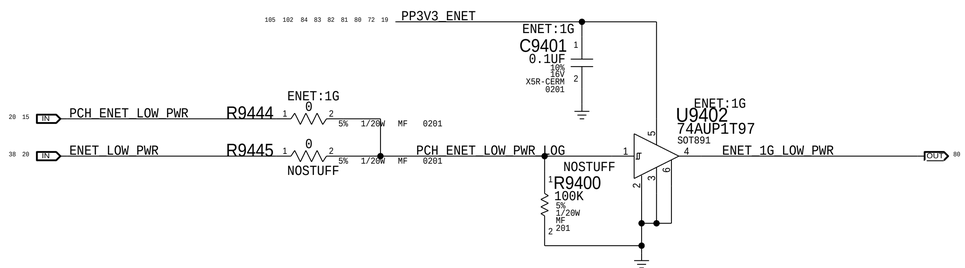
CAESAR IV 1.2V INT.VR CMPTS



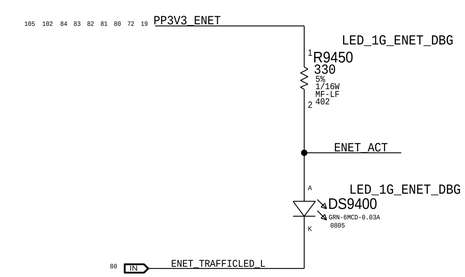
Misc Alias



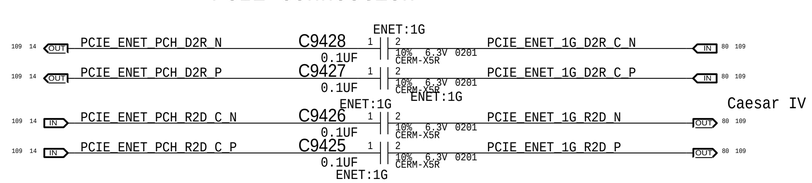
1G ENET LOW PWR



1G ETHERNET ACTIVITY LED



PCIE Connection



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PAGE TITLE
1G ENET SUPPORT

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DRAWING NUMBER	051-02424
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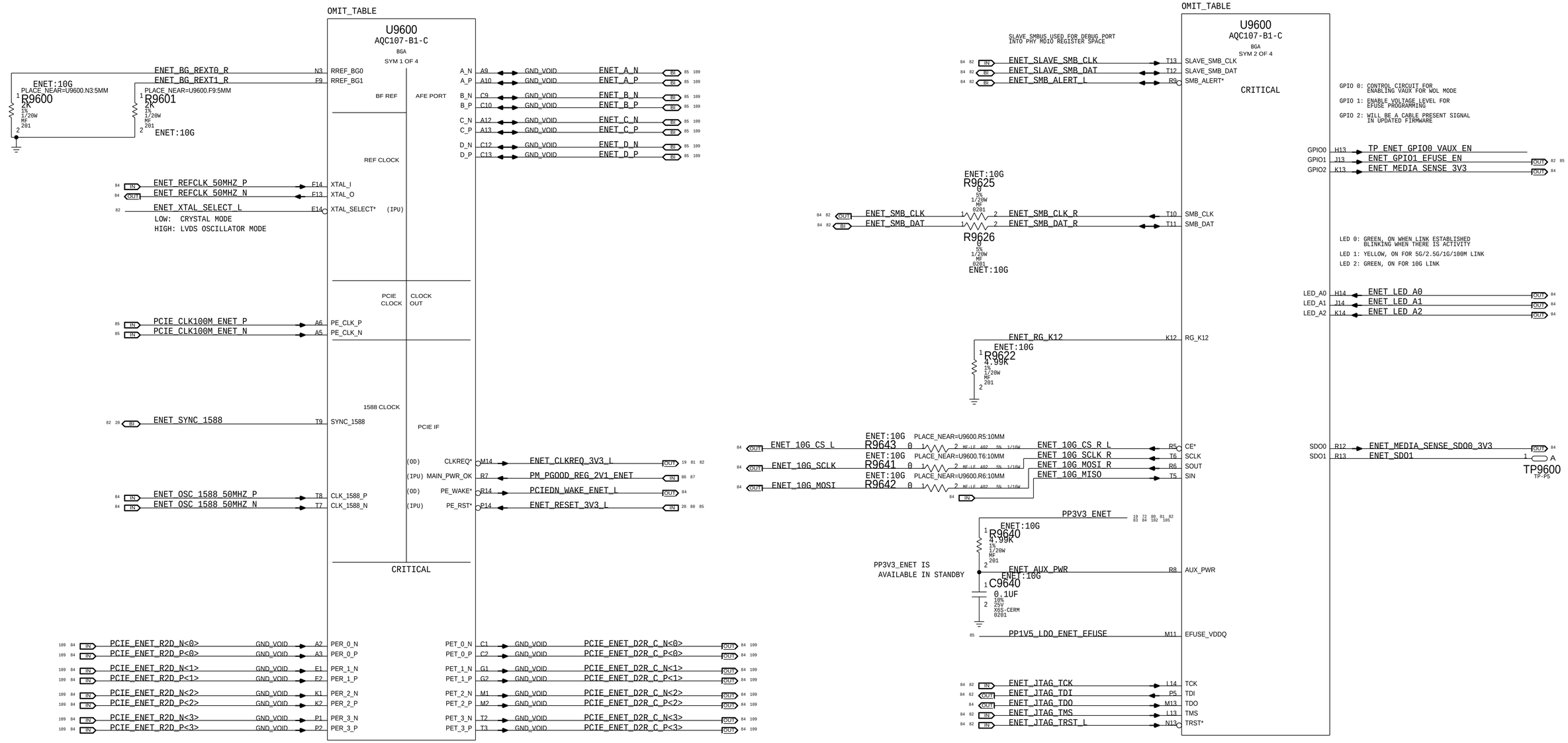
OMIT_TABLE
U9600
AQC107-B1-C
BGA
SYM 1 OF 4
ENET:10G
PLACE_NEAR=U9600.N3:5MM
R9600
2K
1%
1/20W
MF
201
PLACE_NEAR=U9600.F9:5MM
R9601
2K
1%
1/20W
MF
201
ENET:10G
ENET_BG_REXT0_R
ENET_BG_REXT1_R
RREF_BG0
RREF_BG1
BF REF
AFE PORT
REF CLOCK
ENET_REFCLK_50MHZ_P
ENET_REFCLK_50MHZ_N
XTAL_I
XTAL_O
ENET_XTAL_SELECT_L
XTAL_SELECT* (IPU)
LOW: CRYSTAL MODE
HIGH: LVDS OSCILLATOR MODE
PCIE CLOCK
CLOCK OUT
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
PE_CLK_P
PE_CLK_N
1588 CLOCK
ENET_SYNC_1588
SYNC_1588
PCIE IF
CLKREQ*
MAIN_PWR_OK
PE_WAKE*
PE_RST*
ENET_CLKREQ_3V3_L
PM_PGOOD_REG_2V1_ENET
PCIEDN_WAKE_ENET_L
ENET_RESET_3V3_L
ENET_OSC_1588_50MHZ_P
ENET_OSC_1588_50MHZ_N
CLK_1588_P
CLK_1588_N
CRITICAL
A_N
A_P
B_N
B_P
C_N
C_P
D_N
D_P
GND_VOID
ENET_A_N
ENET_A_P
ENET_B_N
ENET_B_P
ENET_C_N
ENET_C_P
ENET_D_N
ENET_D_P
PCIE_ENET_R2D_N<0>
PCIE_ENET_R2D_P<0>
PCIE_ENET_R2D_N<1>
PCIE_ENET_R2D_P<1>
PCIE_ENET_R2D_N<2>
PCIE_ENET_R2D_P<2>
PCIE_ENET_R2D_N<3>
PCIE_ENET_R2D_P<3>
PER_0_N
PER_0_P
PER_1_N
PER_1_P
PER_2_N
PER_2_P
PER_3_N
PER_3_P
PET_0_N
PET_0_P
PET_1_N
PET_1_P
PET_2_N
PET_2_P
PET_3_N
PET_3_P
PCIE_ENET_D2R_C_N<0>
PCIE_ENET_D2R_C_P<0>
PCIE_ENET_D2R_C_N<1>
PCIE_ENET_D2R_C_P<1>
PCIE_ENET_D2R_C_N<2>
PCIE_ENET_D2R_C_P<2>
PCIE_ENET_D2R_C_N<3>
PCIE_ENET_D2R_C_P<3>
OMIT_TABLE
U9600
AQC107-B1-C
BGA
SYM 2 OF 4
SLAVE SMBUS USED FOR DEBUG PORT
INTO PHY MDIO REGISTER SPACE
ENET_SLAVE_SMB_CLK
ENET_SLAVE_SMB_DAT
ENET_SMB_ALERT_L
SLAVE_SMB_CLK
SLAVE_SMB_DAT
SMB_ALERT*
CRITICAL
GPIO 0: CONTROL CIRCUIT FOR
ENABLING VAUX FOR WOL MODE
GPIO 1: ENABLE VOLTAGE LEVEL FOR
EFUSE PROGRAMMING
GPIO 2: WILL BE A CABLE PRESENT SIGNAL
IN UPDATED FIRMWARE
GPIO0
GPIO1
GPIO2
TP_ENET_GPIO0_VAUX_EN
ENET_GPIO1_EFUSE_EN
ENET_MEDIA_SENSE_3V3
ENET:10G
R9625
0
5%
1/20W
MF
0201
R9626
0
5%
1/20W
MF
0201
ENET:10G
ENET_SMB_CLK
ENET_SMB_DAT
ENET_SMB_CLK_R
ENET_SMB_DAT_R
SMB_CLK
SMB_DAT
LED 0: GREEN, ON WHEN LINK ESTABLISHED
BLINKING WHEN THERE IS ACTIVITY
LED 1: YELLOW, ON FOR 5G/2.5G/1G/100M LINK
LED 2: GREEN, ON FOR 10G LINK
LED_A0
LED_A1
LED_A2
ENET_LED_A0
ENET_LED_A1
ENET_LED_A2
ENET_RG_K12
RG_K12
ENET:10G
R9622
4.99K
1%
1/20W
MF
201
ENET:10G PLACE_NEAR=U9600.R5:10MM
R9643 0 1 2 MF-LF 402 5% 1/16W
ENET:10G PLACE_NEAR=U9600.T6:10MM
R9641 0 1 2 MF-LF 402 5% 1/16W
ENET:10G PLACE_NEAR=U9600.R6:10MM
R9642 0 1 2 MF-LF 402 5% 1/16W
ENET_10G_CS_L
ENET_10G_SCLK
ENET_10G_MOSI
ENET_10G_CS_R_L
ENET_10G_SCLK_R
ENET_10G_MOSI_R
ENET_10G_MISO
CE*
SCLK
SOUT
SIN
SDO0
SDO1
ENET_MEDIA_SENSE_SDO0_3V3
ENET_SDO1
TP9600
TP-P5
PP3V3_ENET
ENET:10G
R9640
4.99K
1%
1/20W
MF
201
PP3V3_ENET IS
AVAILABLE IN STANDBY
ENET_AUX_PWR
AUX_PWR
ENET:10G
C9640
0.1UF
10%
25V
X6S-CERM
0201
PP1V5_LDO_ENET_EFUSE
EFUSE_VDDQ
ENET_JTAG_TCK
ENET_JTAG_TDI
ENET_JTAG_TDO
ENET_JTAG_TMS
ENET_JTAG_TRST_L
TCK
TDI
TDO
TMS
TRST*
PULL UPS
PP3V3_ENET
R9689 4.99K ENET_CLKREQ_3V3_L
R9690 4.99K ENET:10G ENET_SMB_CLK
R9691 4.99K ENET:10G ENET_SMB_DAT
R9692 4.99K NOSTUFF ENET_SLAVE_SMB_CLK
R9693 4.99K NOSTUFF ENET_SLAVE_SMB_DAT
R9694 1K NOSTUFF ENET_JTAG_TMS
R9695 1K NOSTUFF ENET_JTAG_TDI
PP3V3_S5
R9686 4.99K NOSTUFF ENET_SYNC_1588
PULL UP / DOWNS
PP3V3_ENET
R9699 4.99K ENET:10G ENET_SMB_ALERT_L
R9698 4.99K NOSTUFF
R9612 4.99K ENET_REFCLK:OSC ENET_XTAL_SELECT_L
R9610 0 ENET_REFCLK:CRYSTAL
PULL DOWNS
R9697 1K NOSTUFF ENET_JTAG_TCK
R9688 4.99K ENET:10G ENET_JTAG_TRST_L
R9611 0 NOSTUFF ENET_SYNC_1588
R9613 10K ENET:10G ENET_GPIO1_EFUSE_EN
BOM_COST_GROUP=ETHERNET
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
10G ETHERNET CONTROLLER 1
Apple Inc.
DRAWING NUMBER
051-02424
SIZE
D
REVISION
6.0.0
BRANCH
dvt-1
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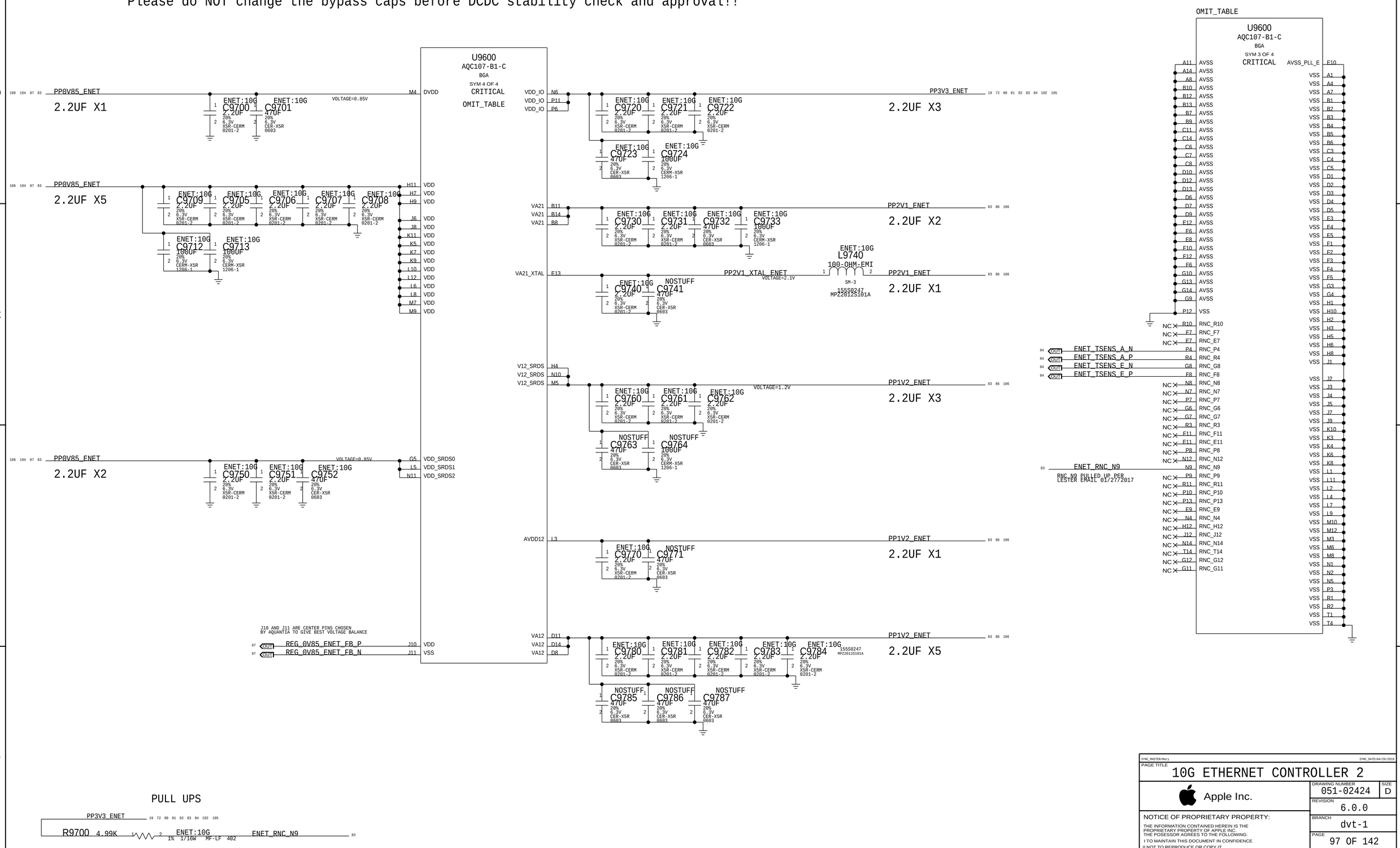
Please do NOT change the bypass caps before DCDC stability check and approval!!



SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

10G ETHERNET CONTROLLER 2

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

BRANCH dvt-1

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R2D ETHERNET PCIE CAPS

PCIE_ENET_R2D_C_N<0> — C9840 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_N<0>
PCIE_ENET_R2D_C_P<0> — C9841 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_P<0>
PCIE_ENET_R2D_C_N<1> — C9842 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_N<1>
PCIE_ENET_R2D_C_P<1> — C9843 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_P<1>
PCIE_ENET_R2D_C_N<2> — C9844 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_N<2>
PCIE_ENET_R2D_C_P<2> — C9845 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_P<2>
PCIE_ENET_R2D_C_N<3> — C9846 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_N<3>
PCIE_ENET_R2D_C_P<3> — C9847 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_R2D_P<3>

D2R ETHERNET PCIE CAPS

PCIE_ENET_D2R_C_N<0> — C9850 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_N<0>
PCIE_ENET_D2R_C_P<0> — C9851 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_P<0>
PCIE_ENET_D2R_C_N<1> — C9852 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_N<1>
PCIE_ENET_D2R_C_P<1> — C9853 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_P<1>
PCIE_ENET_D2R_C_N<2> — C9854 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_N<2>
PCIE_ENET_D2R_C_P<2> — C9855 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_P<2>
PCIE_ENET_D2R_C_N<3> — C9856 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_N<3>
PCIE_ENET_D2R_C_P<3> — C9857 0.1UF 0201 X7R 6.3V 10% ENET:10G — PCIE_ENET_D2R_P<3>

1588 EXTERNAL LVDS OSCILLATOR

PP3V3_ENET — L9860 ENET:10G FERR-600-OHM-2A 0805 — PP3V3_G3H_1588_OSC (VOLTAGE=3.3V)
C9860 2.2UF 20% 6.3V X5R-CERM 0201-2 ENET:10G
R9866 0 5% 1/16W MF-LF 402 ENET:10G
C9861 47UF 20% 6.3V CER-X5R 0603 ENET:10G
C9862 0.1UF 10% 6.3V X7R 0201 ENET:10G
U9860 50MHZ-50PPM-3.3V 5.00X3.20-SM ENET:10G (VDD, OE, OUT, NC, GND)
OSC_1588_OE
OSC_1588_50MHZ_P — R9864 NOSTUFF 1/16W 5% MF-LF 402 — ENET_OSC_1588_50MHZ_P
OSC_1588_50MHZ_N — R9865 NOSTUFF 1/16W 5% MF-LF 402 — ENET_OSC_1588_50MHZ_N

FLASH MEMORY

PP3V3_ENET
R9890 1K 5% 1/16W MF-LF 402 ENET:10G
R9891 1K 5% 1/16W MF-LF 402 ENET:10G
R9892 4.99K 1% 1/20W MF 201 ENET:10G
C9890 1.0UF 10% 25V X6S 0402 ENET:10G
U9890 32MB-85MHZ-2.3V-3.6V SOIC CRITICAL AT45DB321E OMIT_TABLE (VCC, SCK, CS*, WP*, RESET*, SI, SO, GND)
ENET_10G_SCLK
ENET_10G_CS_L
ENET_10G_SPI_WP_L
ENET_10G_SPI_RST_L
ENET_10G_MOSI
ENET_10G_MISO_R — R9893 ENET:10G 1/16W 5% MF-LF 402 PLACE_NEAR=U9890.8:5MM — ENET_10G_MISO

JTAG TPS

ENET_JTAG_TRST_L — TP9820
ENET_JTAG_TDI — TP9821
ENET_JTAG_TCK — TP9822
ENET_JTAG_TMS — TP9823
ENET_JTAG_TDO — TP9824

ETHERNET ACTIVITY LEDS

PP3V3_ENET
R9830 390 5% 1/16W MF-LF 402 DEBUG_LEDS:10G — ENET0_LED — DS9830 GRN-SMCD-0.03A 0805 — ENET_LED_A0
R9831 390 5% 1/16W MF-LF 402 DEBUG_LEDS:10G — ENET1_LED — DS9831 AMBER-0805NM-35-56MCD LTST-C281KFKT-5M — ENET_LED_A1
R9832 390 5% 1/16W MF-LF 402 DEBUG_LEDS:10G — ENET2_LED — DS9832 GRN-SMCD-0.03A 0805 — ENET_LED_A2

AQC ON-DIE THERMAL SENSE (TIED)

ENET_TSENS_A_N — R9860 NOSTUFF 1/16W 5% MF-LF 402 NO_XNET_CONNECTION=1
ENET_TSENS_E_N — R9861 0 1/16W 5% MF-LF 402 ENET:10G NO_XNET_CONNECTION=1 — ENET_TSENS_N
ENET_TSENS_A_P — R9862 NOSTUFF 1/16W 5% MF-LF 402 NO_XNET_CONNECTION=1
ENET_TSENS_E_P — R9863 0 1/16W 5% MF-LF 402 ENET:10G NO_XNET_CONNECTION=1 — ENET_TSENS_P

SPARE MOSFET

NC_MEDIA_SENSE_SF_G
NC_MEDIA_SENSE_SF_S
NC_MEDIA_SENSE_SF_D
Q9880 DMN5L06VK-7 SOT563 VER 5 VTH MAX IS 1.0 V

ENET WAKE LEVEL SHIFTER

PP3V3_ENET
R9820 47K 5% 1/20W MF 201
R9821 47K 5% 1/20W MF 201 — PCIEDN_WAKE
MAKE_BASE=TRUE
PCIEDN_WAKE_ENET_L
PCIEDN_WAKE_ENET_L
Q9820 DMN5L06VK-7 SOT563 VER 4 VTH MAX IS 1.0 V OMIT_TABLE
PP1V8_SLPS2R
R9822 NOSTUFF 47K 5% 1/20W MF 201 ENET WAKE HAS IPU — PCIEDN_WAKE_L
Q9820 DMN5L06VK-7 SOT563 VER 4 VTH MAX IS 1.0 V OMIT_TABLE

50 MHZ REFCLK OSCILLATOR

PP3V3_ENET — L9880 ENET:10G FERR-600-OHM-2A 0805 — PP3V3_G3H_ENET_REFCLK (VOLTAGE=3.3V)
C9880 2.2UF 20% 6.3V X5R-CERM 0201 ENET:10G
R9889 0 5% 1/16W MF-LF 402 ENET:10G
C9881 47UF 20% 6.3V CER-X5R 0603 ENET:10G
C9882 0.1UF 10% 6.3V X7R 0201 ENET:10G
U9880 50MHZ-50PPM-3.3V 5.00X3.20-SM ENET:10G (VDD, OE, OUT, NC, GND)
OSC_REFCLK_OE
ENET_OSC_REFCLK_50MHZ_P — R9808 0 1/20W MF 0201 PLACE_NEAR=R9806.2:1MM — ENET_REFCLK_50MHZ_P
ENET_OSC_REFCLK_50MHZ_N — R9807 0 1/20W MF 0201 PLACE_NEAR=R9805.2:1MM — ENET_REFCLK_50MHZ_N
USE OSCILLATOR BY DEFAULT
ENET_REFCLK:OSC
ENET_REFCLK:CRYSTAL
R9805 0 1/20W 5% MF 0201
R9806 0 1/20W 5% MF 0201
NO_XNET_CONNECTION=1
NO_XNET_CONNECTION=1

50 MHZ REFCLK CRYSTAL

C9800 3.0PF +/-0.25PF 25V NP0-C0G 0201 ENET:10G — ENET_XTALO_R
R9800 0 5% 1/16W MF-LF 402 ENET:10G NO_XNET_CONNECTION=1 — ENET_XTALO
Y9800 50MHZ-45PPM-8PF 2.0X1P6-SM ENET:10G PLACE_NEAR=U9600.F14:5.5MM APN 197S00104
R9801 NOSTUFF 1M 5% 1/16W MF-LF 402 NO_XNET_CONNECTION=1
C9801 3.0PF +/-0.25PF 25V NP0-C0G 0201 ENET:10G — ENET_XTALI

ENET MEDIA SENSE LEVEL SHIFTER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00074	2	dual FET	Q9820,Q2935	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00074	1	dual FET	Q9880	CRITICAL	ENET:1G

ENET_MEDIA_SENSE_3V3 — R9887 NOSTUFF 1/16W 5% MF-LF 402
ENET_MEDIA_SENSE_SD00_3V3 — R9888 NOSTUFF 1/16W 5% MF-LF 402
From Caesar IV — ENET_1G_MEDIA_SENSE — R9899 ENET:1G 1/16W 5% MF-LF 402 — ENET_SENSE_FET_LS
Q9880 DMN5L06VK-7 SOT563 VER 3 VTH MAX IS 1.0 V OMIT_TABLE
PP1V8_SLPS2R
R9885 100K 5% 1/20W MF 201
R9886 30K 5% 1/20W MF 201 — ENET_MEDIA_SENSE

ETHERNET SLAVE SMBUS DEBUG

ENET_SLAVE_SMB_CLK — TP9800
ENET_SLAVE_SMB_DAT — TP9801
TP9802

ETHERNET MULTI-MASTER SMBUS DEBUG

ENET_SMB_ALERT_L — TP9807
ENET_SMB_CLK — TP9805
ENET_SMB_DAT — TP9806
TP9808

LAYOUT NOTE: PLACE TPS AT 0.1MM PITCH IN STRAIGHT ROW IN SAME ORDER SHOWN HERE

BOM_COST_GROUP=ETHERNET

SYNC_MASTER=Mary — SYNC_DATE=04/26/2010

PAGE TITLE: 10G ENET SUPPORT 1

Apple Inc.

DRAWING NUMBER: 051-02424 — SIZE: D
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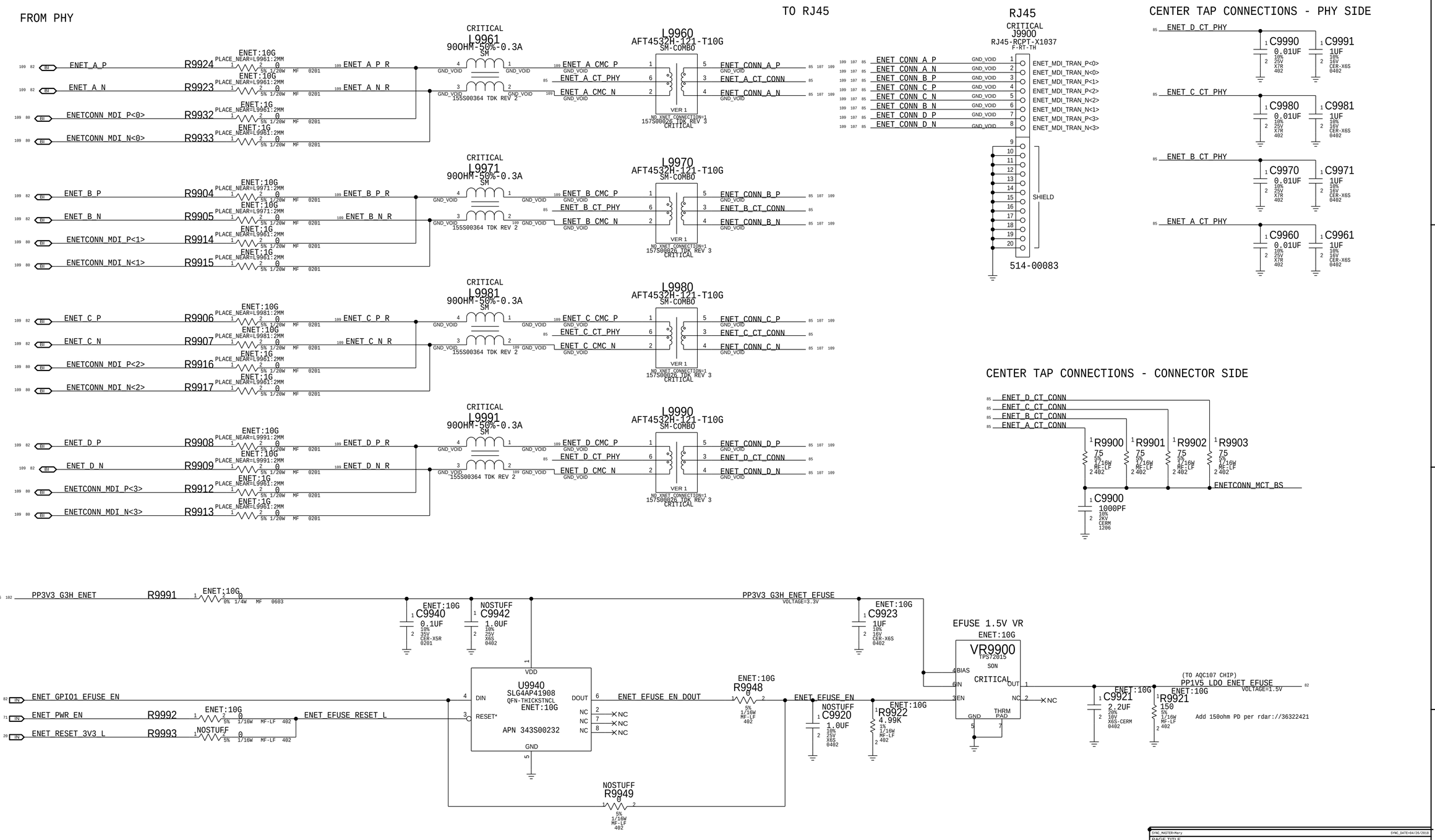

PAGE TITLE
10G ENET SUPPORT 2

Apple Inc.

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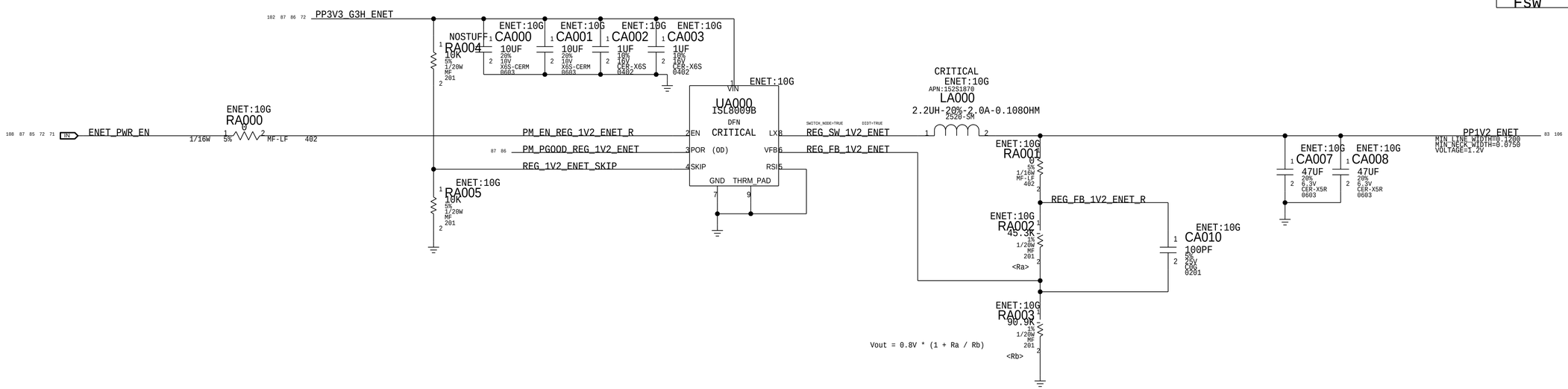
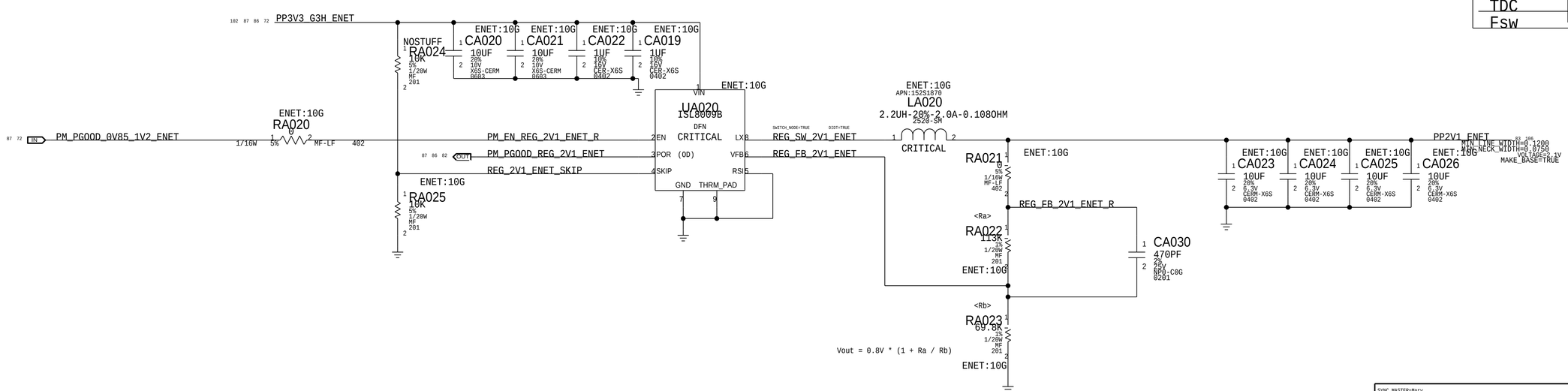
ENET 1V2 REGULATOR	
VOUT	1.20 V
EDC	1 A
OC (TYP)	2.2 A
TDC	0.9 A
Fsw	1.6 MHZ

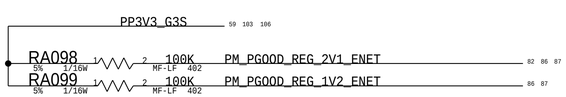
1.2V ENET REGULATOR



ENET 2V1 REGULATOR	
VOUT	2.10 V
EDC	0.5 A
OC (TYP)	2.2 A
TDC	0.4 A
Fsw	1.6 MHZ

2.1V ENET REGULATOR





BOM_COST_GROUP=ETHERNET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: VR 10G ENET 1V2, 2V1

Apple Inc.

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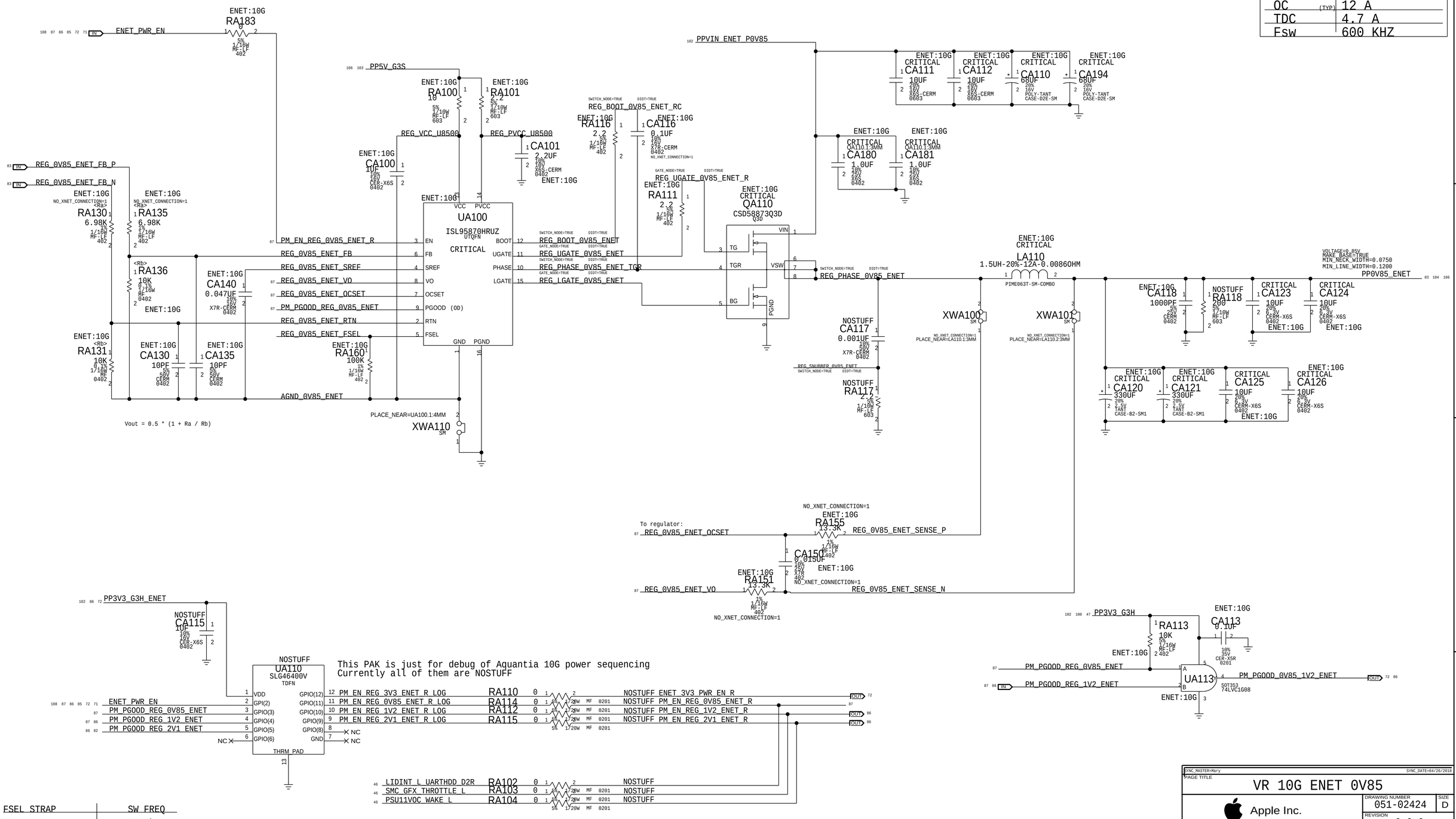
ENET 0V85 REGULATOR	
VOUT	0.85 V
EDC	6.5 A
OC (TYP)	12 A
TDC	4.7 A
Fsw	600 KHZ



This PAK is just for debug of Aquantia 10G power sequencing
Currently all of them are NOSTUFF

ESEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz

BOM_COST_GROUP=ETHERNET

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: VR 10G ENET 0V85

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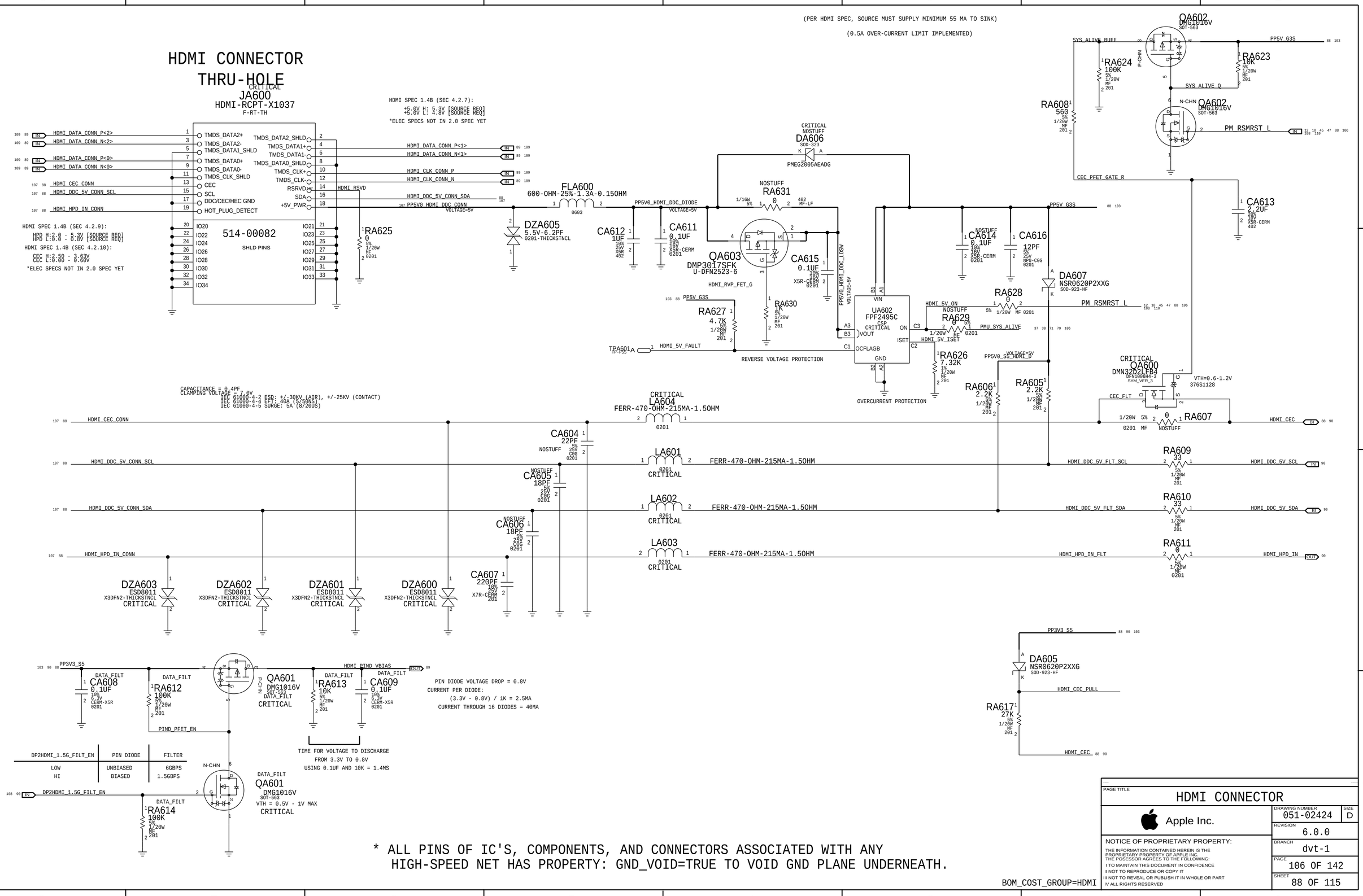
HDMI CONNECTOR
THRU-HOLE
CRITICAL
JA600
HDMI-RCPT-X1037
F-RT-TH
514-00082
SHLD PINS
HDMI SPEC 1.4B (SEC 4.2.7):
+5.0V H: 5.3V [SOURCE REQ]
+5.0V L: 4.8V [SOURCE REQ]
*ELEC SPECS NOT IN 2.0 SPEC YET
HDMI SPEC 1.4B (SEC 4.2.9):
HPD H:2.0 - 5.3V [SOURCE REQ]
HPD L:0.0 - 0.8V [SOURCE REQ]
HDMI SPEC 1.4B (SEC 4.2.10):
CEC H:0.60 - 3.63V
CEC L:0.00 - 0.08V
*ELEC SPECS NOT IN 2.0 SPEC YET
(PER HDMI SPEC, SOURCE MUST SUPPLY MINIMUM 55 MA TO SINK)
(0.5A OVER-CURRENT LIMIT IMPLEMENTED)
FLA600
600-OHM-25%-1.3A-0.150HM
DZA605
5.5V-6.2PF
0201-THICKSTNCL
DA606
PMEG2005AEADG
QA603
DMP3017SFK
U-DFN2523-6
UA602
FPF2495C
CSP
OVERCURRENT PROTECTION
REVERSE VOLTAGE PROTECTION
QA602
DMG1016V
SOT-563
DA607
NSR0620P2XXG
SOD-923-HF
QA600
DMN32D2LFB4
VTH=0.6-1.2V
376S1128
CAPACITANCE = 0.4PF
CLAMPING VOLTAGE = 7.0V
IEC 61000-4-2 ESD: +/-30KV (AIR), +/-25KV (CONTACT)
IEC 61000-4-4 EFT: 40A (5/50NS)
IEC 61000-4-5 SURGE: 5A (8/20US)
LA604
FERR-470-OHM-215MA-1.5OHM
LA601
LA602
LA603
DZA603
DZA602
DZA601
DZA600
ESD8011
X3DFN2-THICKSTNCL
QA601
DMG1016V
SOT-563
VTH = 0.5V - 1V MAX
PIN DIODE VOLTAGE DROP = 0.8V
CURRENT PER DIODE:
(3.3V - 0.8V) / 1K = 2.5MA
CURRENT THROUGH 16 DIODES = 40MA
TIME FOR VOLTAGE TO DISCHARGE
FROM 3.3V TO 0.8V
USING 0.1UF AND 10K = 1.4MS
DA605
NSR0620P2XXG
SOD-923-HF
DP2HDMI_1.5G_FILT_EN
LOW
HI
UNBIASED
BIASED
6GBPS
1.5GBPS
* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY
HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.
BOM_COST_GROUP=HDMI
PAGE TITLE
HDMI CONNECTOR
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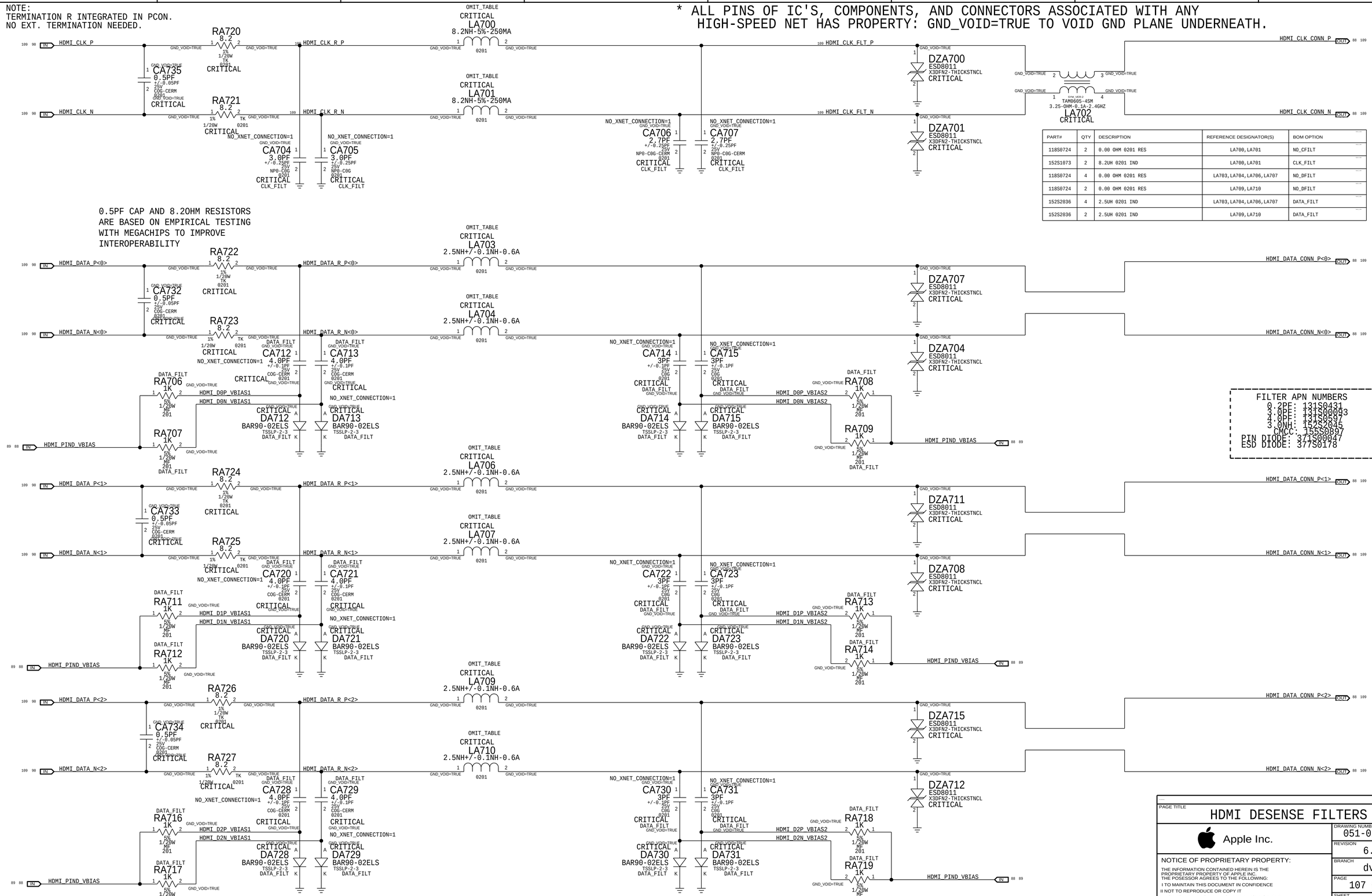
NOTE:
TERMINATION R INTEGRATED IN PCON.
NO EXT. TERMINATION NEEDED.

* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S0724	2	0.00 OHM 0201 RES	LA700,LA701	NO_CFILT
152S1073	2	8.2UH 0201 IND	LA700,LA701	CLK_FILT
118S0724	4	0.00 OHM 0201 RES	LA703,LA704,LA706,LA707	NO_DFILT
118S0724	2	0.00 OHM 0201 RES	LA709,LA710	NO_DFILT
152S2036	4	2.5UH 0201 IND	LA703,LA704,LA706,LA707	DATA_FILT
152S2036	2	2.5UH 0201 IND	LA709,LA710	DATA_FILT

FILTER APN NUMBERS
0.2PF: 131S0431
3.0PF: 131S00093
4.0PF: 131S0597
3.0NH: 152S2045
CMCC: 155S0897
PIN DIODE: 371S00047
ESD DIODE: 377S0178

BOM_COST_GROUP=HDMI

PAGE TITLE
HDMI DESENSE FILTERS

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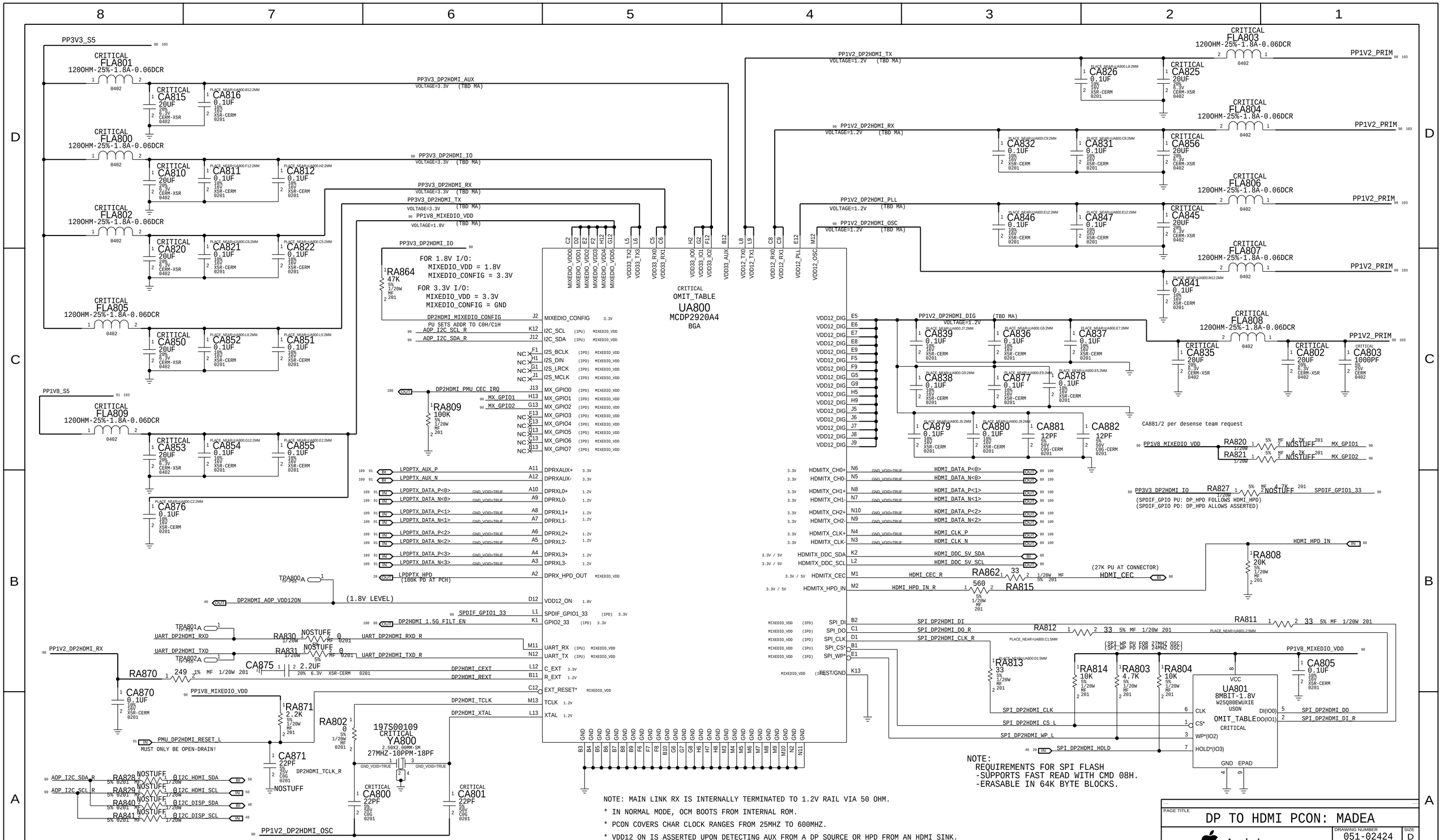

NOTE: MAIN LINK RX IS INTERNALLY TERMINATED TO 1.2V RAIL VIA 50 OHM.

* IN NORMAL MODE, OCM BOOTS FROM INTERNAL ROM.
* PCON COVERS CHAR CLOCK RANGES FROM 25MHZ TO 600MHZ.
* VDD12_ON IS ASSERTED UPON DETECTING AUX FROM A DP SOURCE OR HPD FROM AN HDMI SINK.

CONVERTER MODE:	600MW
SLEEP STATE:	15MW
CS POWER STATE: (TCLK_OFF)	5MW
CS POWER STATE: (VDD12_OFF)	0.1MW

UART (MAX) = 115.2KBPS
I2C (MAX) = 1MBPS (50KBPS)
SPI (MAX) = 75MHZ
INTERNAL OCM CK = 150MHZ
HDMI OUTPUT: 0.25 - 6.0 GBPS

HDMI_TX:
VSWING: 0 - 1200MV
PEMP: 0 - 5DB
DDC = 1 - 100KBPS

1V2	350MA TYPICAL
1V8	5MA TYPICAL
3V3	50MA TYPICAL

BOM_COST_GROUP=HDMI

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
197S00113	197S00109	YA800	CRYSTAL	

PAGE TITLE
DP TO HDMI PCON: MADEA

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 108 OF 142
SHEET 90 OF 115

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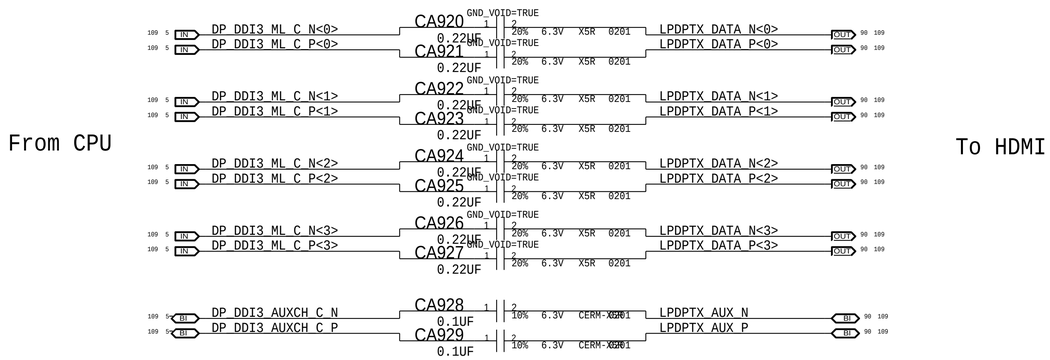
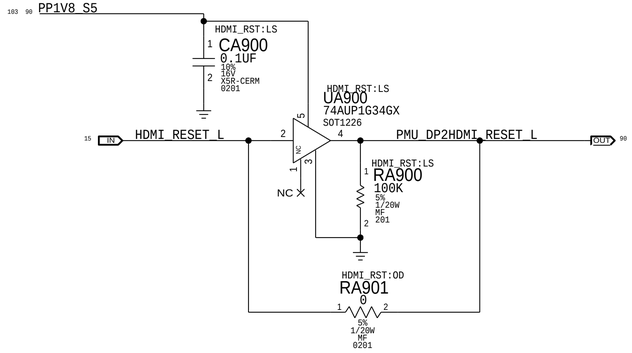
DDI interface AC Caps





BOM_COST_GROUP=HDMI

PAGE TITLE
HDMI PROJECT SUPPORT

Apple Inc.

DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 109 OF 142
SHEET 91 OF 115

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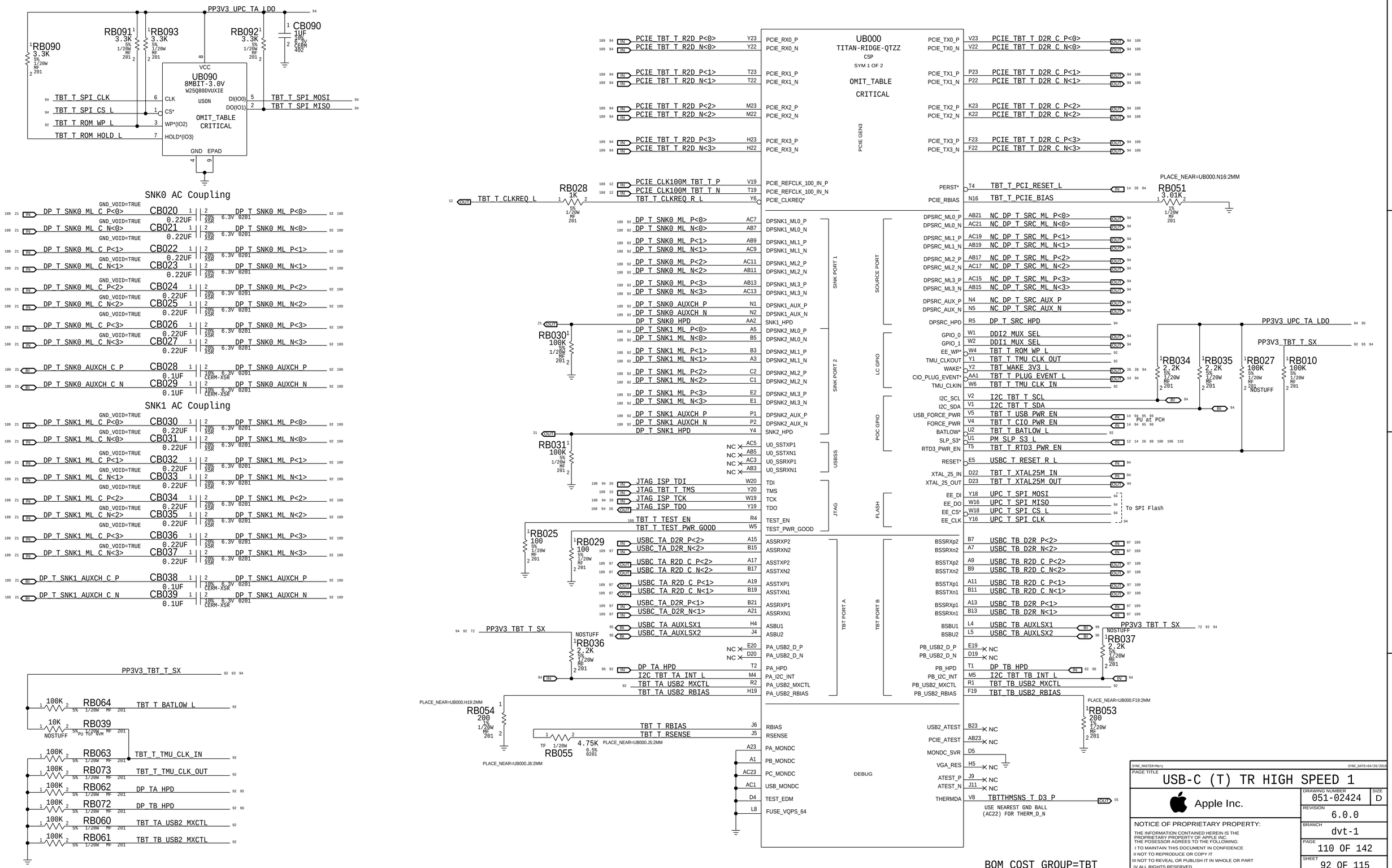
PP3V3_UPC_TA_LDO
RB090 3.3K
RB091 3.3K
RB093 3.3K
RB092 3.3K
CB090 1UF
UB090 8MBIT-3.0V W25Q80DVUXIE USON
OMIT_TABLE CRITICAL
TBT_T_SPI_CLK
TBT_T_SPI_CS_L
TBT_T_ROM_WP_L
TBT_T_ROM_HOLD_L
TBT_T_SPI_MOSI
TBT_T_SPI_MISO
SNK0 AC Coupling
SNK1 AC Coupling
UB000 TITAN-RIDGE-QTZZ CSP SYM 1 OF 2
OMIT_TABLE CRITICAL
PCIE GEN3
SINK PORT 1
SINK PORT 2
SOURCE PORT
LC GPIO
POC GPIO
USBSS
JTAG
FLASH
TBT PORT A
TBT PORT B
DEBUG
TBT_T_CLKREQ_L
RB028 1K
PLACE_NEAR=UB000.N16:2MM
RB051 3.01K
RB030 100K
RB031 100K
RB025 100
RB029 100
RB036 2.2K
RB054 200
RB055 4.75K
RB034 2.2K
RB035 2.2K
RB027 100K
RB010 100K
RB037 2.2K
RB053 200
PU at PCH
To SPI Flash
PP3V3_TBT_T_SX
RB064 100K
RB039 10K
RB063 100K
RB073 100K
RB062 100K
RB072 100K
RB060 100K
RB061 100K
TBT_T_BATLOW_L
TBT_T_TMU_CLK_IN
TBT_T_TMU_CLK_OUT
DP_TA_HPD
DP_TB_HPD
TBT_TA_USB2_MXCTL
TBT_TB_USB2_MXCTL
BOM_COST_GROUP=TBT
USE NEAREST GND BALL (AC22) FOR THERM_D_N
SYNC_MASTER=Mary
SYNC_DATE=04/26/2018
PAGE TITLE
USB-C (T) TR HIGH SPEED 1
Apple Inc.
DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 110 OF 142
SHEET 92 OF 115
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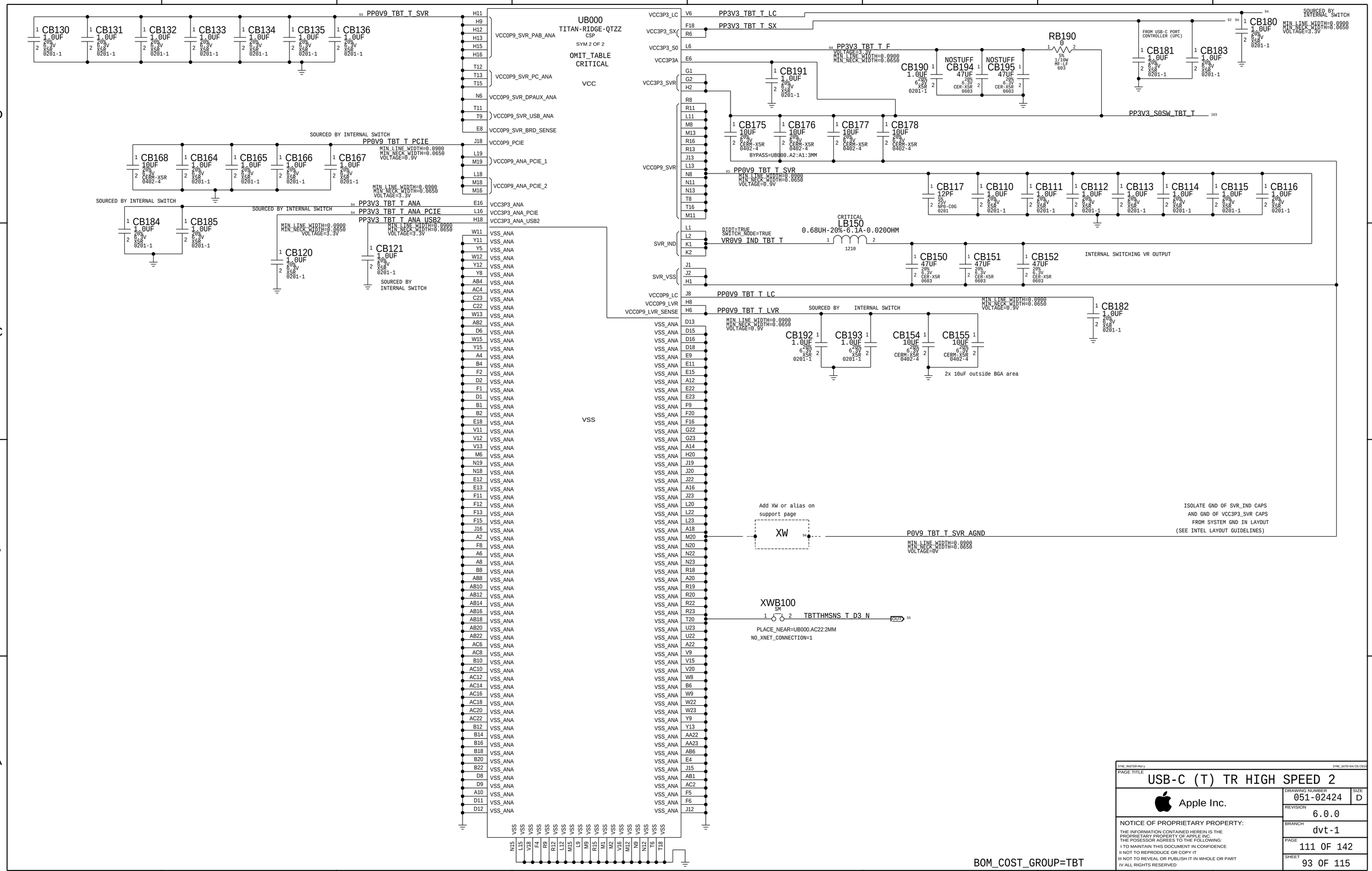

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
USB-C (T) TR HIGH SPEED 2

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

BRANCH dvt-1

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SHEET 93 OF 115

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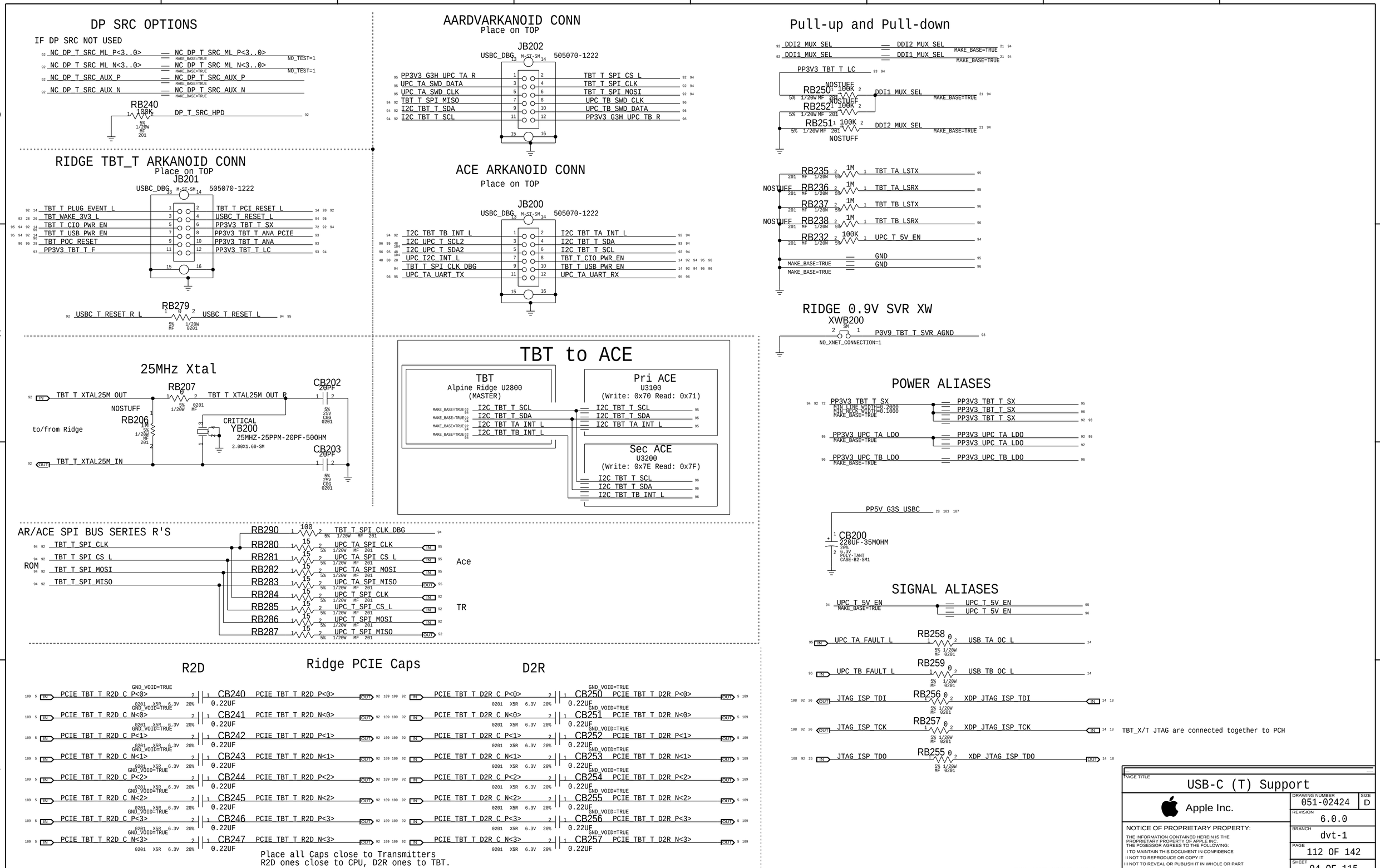
DP SRC OPTIONS
IF DP SRC NOT USED
NC_DP_T_SRC_ML_P<3..0>
NC_DP_T_SRC_ML_N<3..0>
NC_DP_T_SRC_AUX_P
NC_DP_T_SRC_AUX_N
MAKE_BASE=TRUE
NO_TEST=1
RB240 100K
DP_T_SRC_HPD
AARDVARKANOID CONN
Place on TOP
JB202
USBC_DBG M-ST-SM 505070-1222
PP3V3_G3H_UPC_TA_R
UPC_TA_SWD_DATA
UPC_TA_SWD_CLK
TBT_T_SPI_MISO
I2C_TBT_T_SDA
I2C_TBT_T_SCL
TBT_T_SPI_CS_L
TBT_T_SPI_CLK
TBT_T_SPI_MOSI
UPC_TB_SWD_CLK
UPC_TB_SWD_DATA
PP3V3_G3H_UPC_TB_R
Pull-up and Pull-down
DDI2_MUX_SEL
DDI1_MUX_SEL
PP3V3_TBT_T_LC
RB250 100K
RB252 100K
RB251 100K
NOSTUFF
RB235 1M
RB236 1M
RB237 1M
RB238 1M
RB232 100K
TBT_TA_LSTX
TBT_TA_LSRX
TBT_TB_LSTX
TBT_TB_LSRX
UPC_T_5V_EN
GND
RIDGE TBT_T ARKANOID CONN
Place on TOP
JB201
USBC_DBG M-ST-SM 505070-1222
TBT_T_PLUG_EVENT_L
TBT_WAKE_3V3_L
TBT_T_CIO_PWR_EN
TBT_T_USB_PWR_EN
TBT_POC_RESET
PP3V3_TBT_T_F
TBT_T_PCI_RESET_L
USBC_T_RESET_L
PP3V3_TBT_T_SX
PP3V3_TBT_T_ANA_PCIE
PP3V3_TBT_T_ANA
PP3V3_TBT_T_LC
RB279 0
USBC_T_RESET_R_L
USBC_T_RESET_L
ACE ARKANOID CONN
Place on TOP
JB200
USBC_DBG M-ST-SM 505070-1222
I2C_TBT_TB_INT_L
I2C_UPC_T_SCL2
I2C_UPC_T_SDA2
UPC_I2C_INT_L
TBT_T_SPI_CLK_DBG
UPC_TA_UART_TX
I2C_TBT_TA_INT_L
I2C_TBT_T_SDA
I2C_TBT_T_SCL
TBT_T_CIO_PWR_EN
TBT_T_USB_PWR_EN
UPC_TA_UART_RX
RIDGE 0.9V SVR XW
XWB200
P0V9_TBT_T_SVR_AGND
NO_XNET_CONNECTION=1
25MHz Xtal
TBT_T_XTAL25M_OUT
TBT_T_XTAL25M_OUT_R
TBT_T_XTAL25M_IN
RB207 0
RB206 1M
CB202 20PF
CB203 20PF
CRITICAL
YB200
25MHZ-25PPM-20PF-50OHM
2.00X1.60-SM
to/from Ridge
TBT to ACE
TBT
Alpine Ridge U2800
(MASTER)
Pri ACE
U3100
(Write: 0x70 Read: 0x71)
Sec ACE
U3200
(Write: 0x7E Read: 0x7F)
I2C_TBT_T_SCL
I2C_TBT_T_SDA
I2C_TBT_TA_INT_L
I2C_TBT_TB_INT_L
POWER ALIASES
PP3V3_TBT_T_SX
PP3V3_UPC_TA_LDO
PP3V3_UPC_TB_LDO
PP5V_G3S_USBC
CB200 220UF-35MOHM
AR/ACE SPI BUS SERIES R'S
ROM
TBT_T_SPI_CLK
TBT_T_SPI_CS_L
TBT_T_SPI_MOSI
TBT_T_SPI_MISO
RB290 100
RB280 15
RB281 15
RB282 15
RB283 15
RB284 15
RB285 15
RB286 15
RB287 15
TBT_T_SPI_CLK_DBG
UPC_TA_SPI_CLK
UPC_TA_SPI_CS_L
UPC_TA_SPI_MOSI
UPC_TA_SPI_MISO
UPC_T_SPI_CLK
UPC_T_SPI_CS_L
UPC_T_SPI_MOSI
UPC_T_SPI_MISO
Ace
TR
SIGNAL ALIASES
UPC_T_5V_EN
UPC_TA_FAULT_L
UPC_TB_FAULT_L
JTAG_ISP_TDI
JTAG_ISP_TCK
JTAG_ISP_TDO
RB258 0
RB259 0
RB256 0
RB257 0
RB255 0
USB_TA_OC_L
USB_TB_OC_L
XDP_JTAG_ISP_TDI
XDP_JTAG_ISP_TCK
XDP_JTAG_ISP_TDO
TBT_X/T JTAG are connected together to PCH
R2D
Ridge PCIE Caps
D2R
PCIE_TBT_T_R2D_C_P<0>
PCIE_TBT_T_R2D_C_N<0>
PCIE_TBT_T_R2D_C_P<1>
PCIE_TBT_T_R2D_C_N<1>
PCIE_TBT_T_R2D_C_P<2>
PCIE_TBT_T_R2D_C_N<2>
PCIE_TBT_T_R2D_C_P<3>
PCIE_TBT_T_R2D_C_N<3>
PCIE_TBT_T_R2D_P<0>
PCIE_TBT_T_R2D_N<0>
PCIE_TBT_T_R2D_P<1>
PCIE_TBT_T_R2D_N<1>
PCIE_TBT_T_R2D_P<2>
PCIE_TBT_T_R2D_N<2>
PCIE_TBT_T_R2D_P<3>
PCIE_TBT_T_R2D_N<3>
PCIE_TBT_T_D2R_C_P<0>
PCIE_TBT_T_D2R_C_N<0>
PCIE_TBT_T_D2R_C_P<1>
PCIE_TBT_T_D2R_C_N<1>
PCIE_TBT_T_D2R_C_P<2>
PCIE_TBT_T_D2R_C_N<2>
PCIE_TBT_T_D2R_C_P<3>
PCIE_TBT_T_D2R_C_N<3>
PCIE_TBT_T_D2R_P<0>
PCIE_TBT_T_D2R_N<0>
PCIE_TBT_T_D2R_P<1>
PCIE_TBT_T_D2R_N<1>
PCIE_TBT_T_D2R_P<2>
PCIE_TBT_T_D2R_N<2>
PCIE_TBT_T_D2R_P<3>
PCIE_TBT_T_D2R_N<3>
CB240 0.22UF
CB241 0.22UF
CB242 0.22UF
CB243 0.22UF
CB244 0.22UF
CB245 0.22UF
CB246 0.22UF
CB247 0.22UF
CB250 0.22UF
CB251 0.22UF
CB252 0.22UF
CB253 0.22UF
CB254 0.22UF
CB255 0.22UF
CB256 0.22UF
CB257 0.22UF
Place all Caps close to Transmitters
R2D ones close to CPU, D2R ones to TBT.
BOM_COST_GROUP=USB-C
PAGE TITLE
USB-C (T) Support
Apple Inc.
DRAWING NUMBER
051-02424
SIZE
D
REVISION
6.0.0
BRANCH
dvt-1
PAGE
112 OF 142
SHEET
94 OF 115
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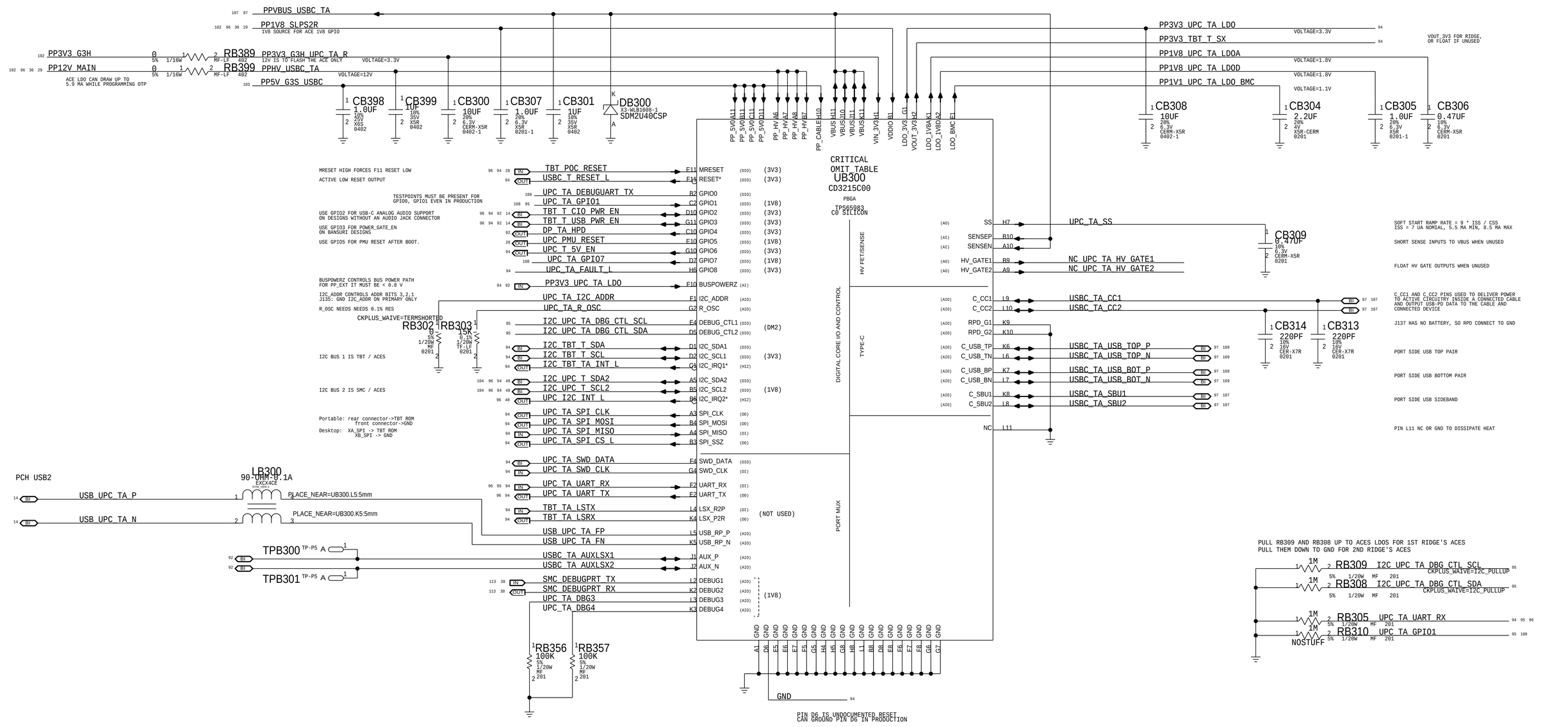
T PRIMARY ACE USB-C PORT CONTROLLER (UPC)

J137 USBC SUPPORTS 5V @ 3A
PP12V IS FOR PROGRAMMING ACE ONLY



NOTE:
DEBUG MUX IS CONNECTED TO PRIMARY ACE OF 1ST RIDGE (XA ACE)
R3752-R3755, R3790-R3792 ARE OPTIONAL

04/26/2018 Mary
NOT SYNCED TO OTHER PLATFORMS

PAGE_TITLE=USB-C (T) PORT CONTROLLER A

BOM_COST_GROUP=USB-C

Apple Inc.

PAGE TITLE	USB-C (T) PORT CONTROLLER A
DRAWING NUMBER	051-02424
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
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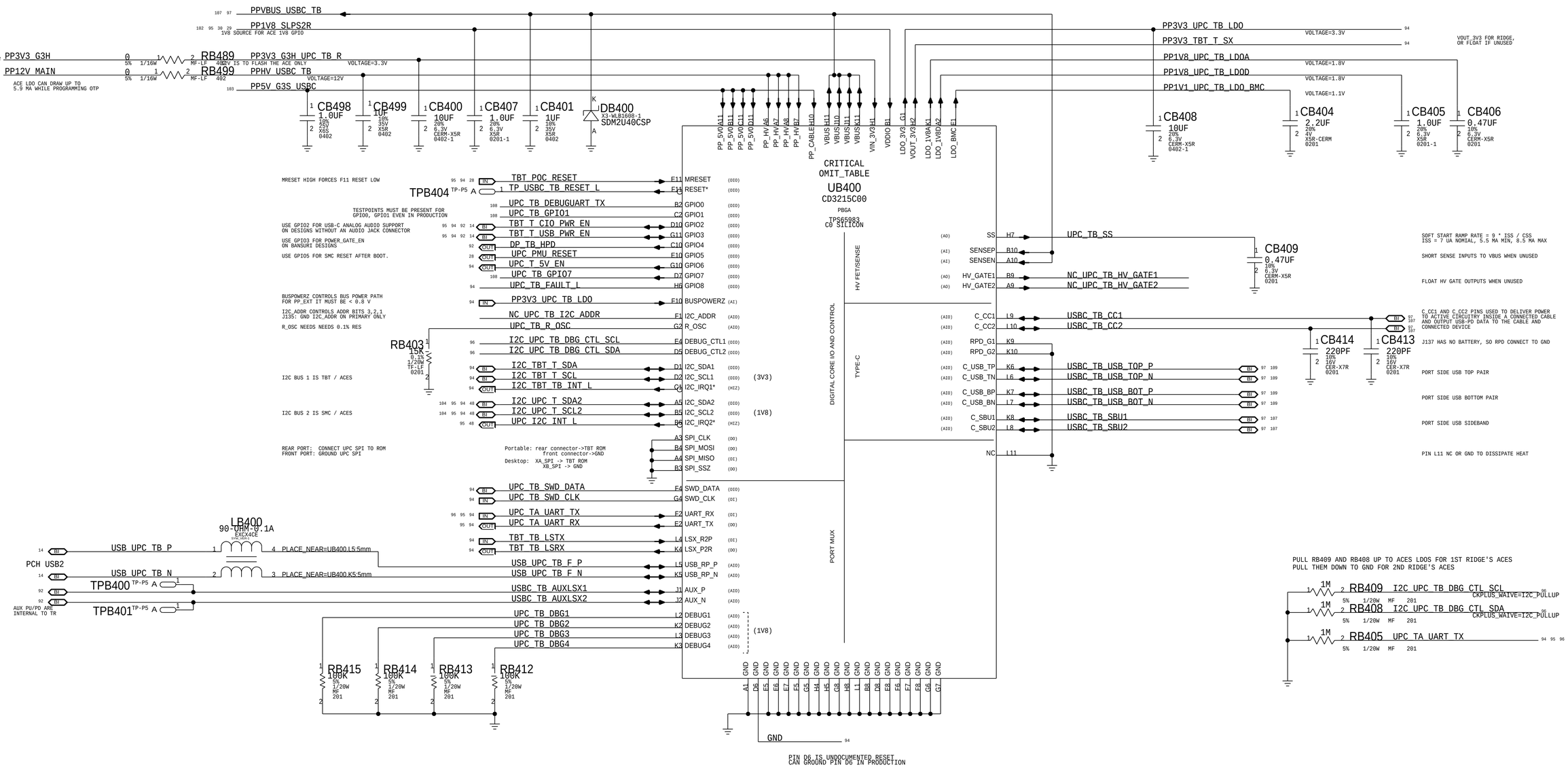
T SECONDARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

NOT SYNCED TO OTHER PLATFORMS
Mary
SYNC_DATE=04/26/2018

PAGE TITLE	PAGE_TITLE=USB-C (T) PORT CONTROLLER B
Apple Inc.	DRAWING NUMBER 051-02424 SIZE D
	REVISION 6.0.0
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	PAGE 114 OF 142
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J137 HAS A QUAD-PACK USB-C CONNECTOR
J137 SUPPORTS 5V @ 3A

PPVBUS_USBC_TA
VOLTAGE=5V
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750

NOSTUFF CB504 1UF 10% 25V X5R 402
DZB500 1610 ESDA25P35-1U1M
CB500 0.01UF 10% 25V X5R-CERM 0201
CB501 0.01UF 10% 25V X5R-CERM 0201
CB502 0.01UF 10% 25V X5R-CERM 0201
CB503 0.01UF 10% 25V X5R-CERM 0201
CB510 1UF 10% 25V X5R 402
PLACE VBUS CAPS NEAR EACH VBUS PIN
CB506 0.01UF 10% 25V X5R-CERM 0201
CB507 0.01UF 10% 25V X5R-CERM 0201
CB508 0.01UF 10% 25V X5R-CERM 0201
CB509 0.01UF 10% 25V X5R-CERM 0201
CB511 3PF +/-0.1PF 25V C0G 0201
CB512 12PF 5% 50V C0G-CERM 0201

USBC_TA_D2R_P<2> — RB570 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TA_D2R_RC_P<2> — CB570 0.33UF 25V 10% CER-X5R 0201 GND_VOID — USBC_TA_D2R_CONN_P<2>
USBC_TA_D2R_N<2> — RB571 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TA_D2R_RC_N<2> — CB571 0.33UF 25V 10% CER-X5R 0201 GND_VOID — USBC_TA_D2R_CONN_N<2>
USBC_TA_SBU1
USBC_TA_USB_TOP_N
USBC_TA_USB_TOP_P
USBC_TA_CC1
USBC_TA_R2D_C_N<1> — RB572 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TA_R2D_RC_N<1> — CB572 0.22UF 25V 10% X5R 0201 GND_VOID — USBC_TA_R2D_CONN_N<1>
USBC_TA_R2D_C_P<1> — RB573 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TA_R2D_RC_P<1> — CB573 0.22UF 25V 10% X5R 0201 GND_VOID — USBC_TA_R2D_CONN_P<1>

CONN C
SYM 3 OF 5
CRITICAL
J3300
RCPT-USBC-QUAD-X1037
F-RT-TH

USBC_TA_D2R_CONN_P<1> — CB578 0.33UF 25V 10% CER-X5R 0201 GND_VOID — USBC_TA_D2R_RC_P<1> — RB578 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TA_D2R_P<1>
USBC_TA_D2R_CONN_N<1> — CB579 0.33UF 25V 10% CER-X5R 0201 GND_VOID — USBC_TA_D2R_RC_N<1> — RB579 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TA_D2R_N<1>
USBC_TA_SBU2
USBC_TA_USB_BOT_N
USBC_TA_USB_BOT_P
USBC_TA_CC2
USBC_TA_R2D_CONN_N<2> — CB580 0.22UF 25V 10% X5R 0201 GND_VOID — USBC_TA_R2D_RC_N<2> — RB580 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TA_R2D_C_N<2>
USBC_TA_R2D_CONN_P<2> — CB581 0.22UF 25V 10% X5R 0201 GND_VOID — USBC_TA_R2D_RC_P<2> — RB581 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TA_R2D_C_P<2>

PPVBUS_USBC_TB
VOLTAGE=5V
MIN_LINE_WIDTH=0.1200
MIN_NECK_WIDTH=0.0750

NOSTUFF CB554 1UF 10% 25V X5R 402
DZB501 1610 ESDA25P35-1U1M
CB550 0.01UF 10% 25V X5R-CERM 0201
CB551 0.01UF 10% 25V X5R-CERM 0201
CB552 0.01UF 10% 25V X5R-CERM 0201
CB553 0.01UF 10% 25V X5R-CERM 0201
CB560 1UF 10% 25V X5R 402
PLACE VBUS CAPS NEAR EACH VBUS PIN
CB556 0.01UF 10% 25V X5R-CERM 0201
CB557 0.01UF 10% 25V X5R-CERM 0201
CB558 0.01UF 10% 25V X5R-CERM 0201
CB559 0.01UF 10% 25V X5R-CERM 0201
CB561 3PF +/-0.1PF 25V C0G 0201
CB562 12PF 5% 50V C0G-CERM 0201

USBC_TB_D2R_P<2> — RB574 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TB_D2R_RC_P<2> — CB574 0.33UF 25V 10% CER-X5R 0201 GND_VOID — USBC_TB_D2R_CONN_P<2>
USBC_TB_D2R_N<2> — RB575 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TB_D2R_RC_N<2> — CB575 0.33UF 25V 10% CER-X5R 0201 GND_VOID — USBC_TB_D2R_CONN_N<2>
USBC_TB_SBU1
USBC_TB_USB_TOP_N
USBC_TB_USB_TOP_P
USBC_TB_CC1
USBC_TB_R2D_C_N<1> — RB576 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TB_R2D_RC_N<1> — CB576 0.22UF 25V 10% X5R 0201 GND_VOID — USBC_TB_R2D_CONN_N<1>
USBC_TB_R2D_C_P<1> — RB577 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TB_R2D_RC_P<1> — CB577 0.22UF 25V 10% X5R 0201 GND_VOID — USBC_TB_R2D_CONN_P<1>

SYM 4 OF 5
CONN D
CRITICAL
J3300
RCPT-USBC-QUAD-X1037
F-RT-TH

USBC_TB_D2R_CONN_P<1> — CB582 0.33UF 25V 10% CER-X5R 0201 GND_VOID — USBC_TB_D2R_RC_P<1> — RB582 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TB_D2R_P<1>
USBC_TB_D2R_CONN_N<1> — CB583 0.33UF 25V 10% CER-X5R 0201 GND_VOID — USBC_TB_D2R_RC_N<1> — RB583 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TB_D2R_N<1>
USBC_TB_SBU2
USBC_TB_USB_BOT_N
USBC_TB_USB_BOT_P
USBC_TB_CC2
USBC_TB_R2D_CONN_N<2> — CB584 0.22UF 25V 10% X5R 0201 GND_VOID — USBC_TB_R2D_RC_N<2> — RB584 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TB_R2D_C_N<2>
USBC_TB_R2D_CONN_P<2> — CB585 0.22UF 25V 10% X5R 0201 GND_VOID — USBC_TB_R2D_RC_P<2> — RB585 3.01 1% 1/20W MF 0201 GND_VOID — USBC_TB_R2D_C_P<2>

CRITICAL
J3300
RCPT-USBC-QUAD-X1037
F-RT-TH
SYM 5 OF 5
USB-C SHIELD

BOM_COST_GROUP=USB-C

SYNC_MASTER=Mary SYNC_DATE=04/26/2018
PAGE TITLE
USB-C (T) CONNECTORS

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 115 OF 142
SHEET 97 OF 115

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Place Holder

BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=06/07/2010

PAGE TITLE
EMPTY

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PAGE 116 OF 142
SHEET 98 OF 115

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PAGE TITLE
Empty

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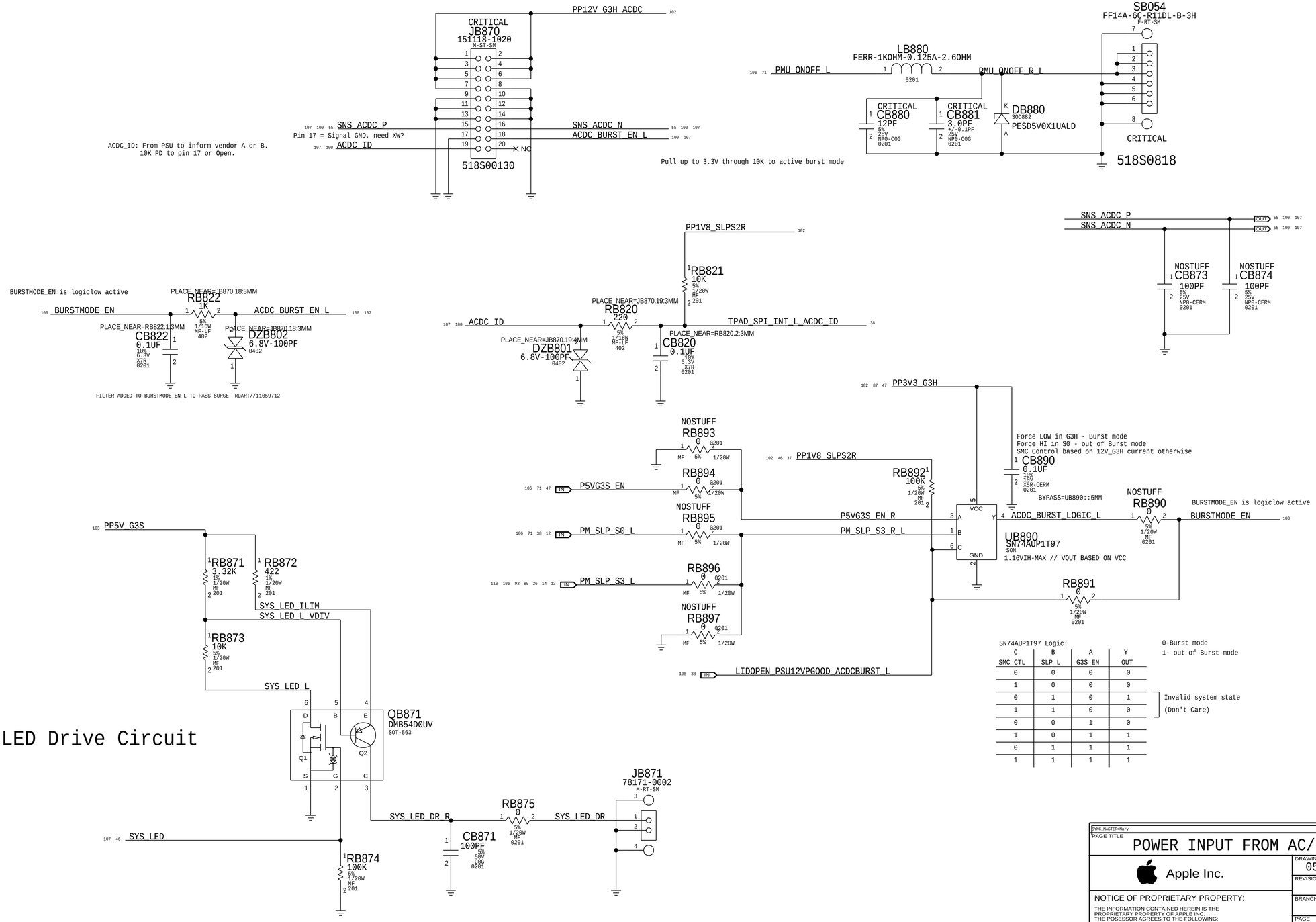
MLB Power button connector



SIL LED Drive Circuit

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE
POWER INPUT FROM AC/DC 1

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PAGE 118 OF 142
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12V PBUS Rails

100 PP12V_G3H_ACDC
- PP12V_G3H_ACDC — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=12V, MAKE_BASE=TRUE — 106
- PP12V_G3H_ACDC — 51
- PP12V_G3H_ACDC — 104

51 PP12V_MAIN
- PP12V_MAIN — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=12V, MAKE_BASE=TRUE — 105 106
- PP12V_MAIN — 63
- PP12V_MAIN — 56
- PP12V_MAIN — 53
- PP12V_MAIN — 71
- PP12V_MAIN — 29 30 95 96
- PP12V_MAIN — 51
- PP12V_MAIN — 51
- PP12V_MAIN — 57
- PP12V_MAIN — 47
- PP12V_MAIN — 104
- PP12V_MAIN — 60

CPU High Side Rails

51 PPBUS_HS_CPU
- PPBUS_HS_CPU — MIN_LINE_WIDTH=0.7000, MIN_NECK_WIDTH=0.0650, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PPBUS_HS_CPU — 63 64 65 66 73
- PPBUS_HS_CPU — 67
- PPBUS_HS_CPU — 104 105

3V3_G3H High Side Rails

51 PP12V_G3H_VIN_P3V3_G3H
- PP12V_G3H_VIN_P3V3_G3H — MIN_LINE_WIDTH=0.1930, MIN_NECK_WIDTH=0.0650, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PP12V_G3H_VIN_P3V3_G3H — 68
- PP12V_G3H_VIN_P3V3_G3H — 104 105

5V_G3S High Side Rails

51 PP12V_G3H_VIN_P5V_G3S
- PP12V_G3H_VIN_P5V_G3S — MIN_LINE_WIDTH=0.1930, MIN_NECK_WIDTH=0.0650, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PP12V_G3H_VIN_P5V_G3S — 68
- PP12V_G3H_VIN_P5V_G3S — 104 105

12V to NAND 2V7 VR Rails

53 PPVIN_G3H_P2V7
- PPVIN_G3H_P2V7 — MIN_LINE_WIDTH=0.3000, MIN_NECK_WIDTH=0.0720, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PPVIN_G3H_P2V7 — 79

12V to ENET VR Rails

56 PPVIN_ENET_P0V85
- PPVIN_ENET_P0V85 — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=12V — 107
- PPVIN_ENET_P0V85 — 87
- PPVIN_ENET_P0V85 — 104

3V3 G3H Rails

68 PP3V3_G3H
- PP3V3_G3H — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 105 106
- PP3V3_G3H — 54
- PP3V3_G3H — 102
- PP3V3_G3H — 54
- PP3V3_G3H — 56
- PP3V3_G3H — 72
- PP3V3_G3H — 72
- PP3V3_G3H — 102
- PP3V3_G3H — 29
- PP3V3_G3H — 30
- PP3V3_G3H — 95
- PP3V3_G3H — 96
- PP3V3_G3H — 47 87 100
- PP3V3_G3H — 53
- PP3V3_G3H — 110
- PP3V3_G3H — 28
- PP3V3_G3H — 67
- PP3V3_G3H — 19
- PP3V3_G3H — 73
- PP3V3_G3H — 70
- PP3V3_G3H — 113
- PP3V3_G3H — 70
- PP3V3_G3H — 113
- PP3V3_G3H — 48
- PP3V3_G3H — 72

3V3_G3H SSD Rail

53 PP3V3_G3H_SSD
- PP3V3_G3H_SSD — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 106
- PP3V3_G3H_SSD — 79 105
- PP3V3_G3H_SSD — 104

CPU Rails

64 PPVCC_S0_CPU_REG
- PPVCC_S0_CPU_REG — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.52V — 106
- PPVCC_S0_CPU_REG — 6 8 56
- PPVCC_S0_CPU_REG — 10
- PPVCC_S0_CPU_REG — 104 105

66 PPVCCSA_S0_CPU_REG
- PPVCCSA_S0_CPU_REG — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.52V — 106
- PPVCCSA_S0_CPU_REG — 8 56
- PPVCCSA_S0_CPU_REG — 11

65 PPVCCGT_S0_CPU_REG
- PPVCCGT_S0_CPU_REG — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.52V — 106
- PPVCCGT_S0_CPU_REG — 8 56
- PPVCCGT_S0_CPU_REG — 10
- PPVCCGT_S0_CPU_REG — 104

CPU VCCIO Rails

54 PPVCCIO_S0_CPU
- PPVCCIO_S0_CPU — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=0.95V — 106
- PPVCCIO_S0_CPU — 5 8
- PPVCCIO_S0_CPU — 11
- PPVCCIO_S0_CPU — 104 105

BUCK0 VDD SoC CPU

69 PPVDDCPU_AWAKE_SOC
- PPVDDCPU_AWAKE_SOC — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.06V — 106
- PPVDDCPU_AWAKE_SOC — 41 105 112

BUCK1 VDD SoC CPU SRAM

69 PPVDDCPUSRAM_AWAKE
- PPVDDCPUSRAM_AWAKE — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.06V — 106
- PPVDDCPUSRAM_AWAKE — 41

BUCK2 SoC VDD_SOC

69 PP0V82_SLPDDR
- PP0V82_SLPDDR — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=.82V — 106
- PP0V82_SLPDDR — 41 105 112

V3P3_SW1 USB

70 PP3V3_AWAKE
- PP3V3_AWAKE — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=3.3V — 106
- PP3V3_AWAKE — 43

PMIC LDO2 PCIE_REFBUF/PLL

70 PP1V2_AWAKE
- PP1V2_AWAKE — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.0750, MAKE_BASE=TRUE, VOLTAGE=1.2V — 106
- PP1V2_AWAKE — 43
- PP1V2_AWAKE — 43
- PP1V2_AWAKE — 43
- PP1V2_AWAKE — 43

PMIC LDO0 - VDD_LOW

70 PP0V8_SLPS2R
- PP0V8_SLPS2R — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=0.8V, MAKE_BASE=TRUE — 106
- PP0V8_SLPS2R — 42

RTC Rails (PMIC LDO 1)

19 PP3V0_G3H_RTC
- PP3V0_G3H_RTC — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3V, MAKE_BASE=TRUE — 106
- PP3V0_G3H_RTC — 12 16 17

Calpe 3V3 VDD Rail

54 PP3V3_G3H_PMU
- PP3V3_G3H_PMU — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 107
- PP3V3_G3H_PMU — 69
- PP3V3_G3H_PMU — 70
- PP3V3_G3H_PMU — 70
- PP3V3_G3H_PMU — 71
- PP3V3_G3H_PMU — 70

3V3_G3H ENET Rail

56 PP3V3_G3H_ENET
- PP3V3_G3H_ENET — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 85 106
- PP3V3_G3H_ENET — 72 86 87

3V3 ENET Rail(Pass FET)

105 84 83 82 81 80 72 19 PP3V3_ENET
- PP3V3_ENET — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.3V, MAKE_BASE=TRUE — 106
- PP3V3_ENET — 104

BUCK3 AOP/SMC/VDD1(1V8)

69 PP1V8_SLPS2R
- PP1V8_SLPS2R — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.8V, MAKE_BASE=TRUE — 84 106
- PP1V8_SLPS2R — 43
- PP1V8_SLPS2R — 43
- PP1V8_SLPS2R — 43
- PP1V8_SLPS2R — 43
- PP1V8_SLPS2R — 113
- PP1V8_SLPS2R — 69 (Buck3_SW input, 1V8 G3S input)
- PP1V8_SLPS2R — 70
- PP1V8_SLPS2R — 71
- PP1V8_SLPS2R — 48
- PP1V8_SLPS2R — 48
- PP1V8_SLPS2R — 48
- PP1V8_SLPS2R — 45
- PP1V8_SLPS2R — 45
- PP1V8_SLPS2R — 37 46 100
- PP1V8_SLPS2R — 29 30 95 96 (1V8_SLPS2R MISC)
- PP1V8_SLPS2R — 110
- PP1V8_SLPS2R — 100

BUCK3_SW1(1V8)

69 PP1V8_AWAKE
- PP1V8_AWAKE — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.8V, MAKE_BASE=TRUE — 106
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 43
- PP1V8_AWAKE — 71
- PP1V8_AWAKE — 45
- PP1V8_AWAKE — 28 40 45 46 (1V8_AWAKE MISC)
- PP1V8_AWAKE — 45
- PP1V8_AWAKE — 113
- PP1V8_AWAKE — 104

BUCK4 SDRAM VDD2 (1V1)

69 PP1V1_SLPS2R
- PP1V1_SLPS2R — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.1V, MAKE_BASE=TRUE — 106
- PP1V1_SLPS2R — 42
- PP1V1_SLPS2R — 43
- PP1V1_SLPS2R — 70 (0V8 LDO0 input)
- PP1V1_SLPS2R — 69 (Buck4_SW input)
- PP1V1_SLPS2R — 70 (1V1 SLPDDR SW input)

1V1 SLPDDR SOC VDDIO DDR (SoC Transition State)

70 PP1V1_SLPDDR
Source from 1V1_SLPS2R
EN by PMIC.GPIO
- PP1V1_SLPDDR — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.1V, MAKE_BASE=TRUE — 106
- PP1V1_SLPDDR — 42 105
- PP1V1_SLPDDR — 37
- PP1V1_SLPDDR — 42
- PP1V1_SLPDDR — 43

BUCK5 VDD_FIXED

69 PP0V9_SLPDDR
- PP0V9_SLPDDR — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=0.9V, MAKE_BASE=TRUE — 106
- PP0V9_SLPDDR — 42 105
- PP0V9_SLPDDR — 42
- PP0V9_SLPDDR — 42
- PP0V9_SLPDDR — 42
- PP0V9_SLPDDR — 42

LDO1 for RTC

70 19 PPVRTC_G3_PCH_REG_R
- PPVRTC_G3_PCH_REG_R — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=3.0V, MAKE_BASE=TRUE

1.1V PRIM FOR XTAL

17 16 PP1V_PRIM_PCH_VCCAXTAL_F
- PP1V_PRIM_PCH_VCCAXTAL_F — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.8V, MAKE_BASE=TRUE

1.1V PRIM FOR PLL

17 16 PP1V_PRIM_PCH_VCCAPLL_F
- PP1V_PRIM_PCH_VCCAPLL_F — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1.8V, MAKE_BASE=TRUE

1.1V PRIM FOR MPHY_PLL

17 16 PP1V_PRIM_PCH_VCCAMPHYPLL_F
- PP1V_PRIM_PCH_VCCAMPHYPLL_F — MIN_LINE_WIDTH=0.1200, MIN_NECK_WIDTH=0.0750, VOLTAGE=1V, MAKE_BASE=TRUE

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
Power Aliases - 1

Apple Inc.

DRAWING NUMBER	SIZE
051-02424	D
REVISION 6.0.0	
BRANCH dvt-1	
PAGE 120 OF 142	
SHEET 102 OF 115	

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1V S5 Rails

```
69 PP1V_PRIM ═══ PP1V_PRIM                    106
                 MIN_LINE_WIDTH=0.0700
                 MIN_NECK_WIDTH=0.0650
                 VOLTAGE=1.0V
                 MAKE_BASE=TRUE
                 ├── PP1V_PRIM                69
                 ├── PP1V_PRIM                16 17
                 ├── PP1V_PRIM                16
                 ├── PP1V_PRIM                16
                 ├── PP1V_PRIM                16
                 ├── PP1V_PRIM                16 17
                 ├── PP1V_PRIM                17
                 ├── PP1V_PRIM                17
                 ├── PP1V_PRIM                17
                 ├── PP1V_PRIM                18
                 ├── PP1V_PRIM                112
                 ├── PP1V_PRIM                47
                 ├── PP1V_PRIM                16
                 └── PP1V_PRIM                104
```

These 3x rails need filter

1V S3 Rails

```
69 PP1V_S3 ═══ PP1V_S3                        106
               MIN_LINE_WIDTH=0.1200
               MIN_NECK_WIDTH=0.0750
               VOLTAGE=1.0V
               MAKE_BASE=TRUE
               ├── PP1V_S3                    8 11 45
               ├── PP1V_S3                    8 11
               ├── PP1V_S3                    71
               ├── PP1V_S3                    63
               ├── PP1V_S3                    6 13 20
               └── PP1V_S3                    45
```

1V2 S5 Rails

```
69 PP1V2_PRIM ═══ PP1V2_PRIM
                  MIN_LINE_WIDTH=0.1200
                  MIN_NECK_WIDTH=0.0750
                  VOLTAGE=1.2V
                  MAKE_BASE=TRUE
                  └── PP1V2_PRIM               90
```

1V2 S3 Rails

```
67 PP1V2_S3 ═══ PP1V2_S3                      106 107
                MIN_LINE_WIDTH=0.1200
                MIN_NECK_WIDTH=0.0750
                VOLTAGE=1.2V
                MAKE_BASE=TRUE
                ├── PP1V2_S3                   23
                ├── PP1V2_S3                   24
                ├── PP1V2_S3                   22
                ├── PP1V2_S3                   67
                ├── PP1V2_S3                   12
                ├── PP1V2_S3                   105
                ├── PP1V2_S3                   8
                ├── PP1V2_S3                   11
                └── PP1V2_S3                   72

72 PP1V2_S0SW ═══ PP1V2_S0SW                   106
                  MIN_LINE_WIDTH=0.1200
                  MIN_NECK_WIDTH=0.0750
                  VOLTAGE=1.2V
                  MAKE_BASE=TRUE
                  └── PP1V2_S0SW               8 11
```

0V6 Rails

```
23 22 PP0V6_S3_MEM_VREFCAA ═══ PP0V6_S3_MEM_VREFCAA
                               MIN_LINE_WIDTH=0.3000
                               MIN_NECK_WIDTH=0.2000
                               VOLTAGE=0.6V
                               MAKE_BASE=TRUE

24 22 PP0V6_S3_MEM_VREFCAB ═══ PP0V6_S3_MEM_VREFCAB
                               MIN_LINE_WIDTH=0.3000
                               MIN_NECK_WIDTH=0.2000
                               VOLTAGE=0.6V
                               MAKE_BASE=TRUE
```

2V5 VPP Rails

```
67 PP2V5_S3 ═══ PP2V5_S3                      107
                MIN_LINE_WIDTH=0.1200
                MIN_NECK_WIDTH=0.0750
                VOLTAGE=2.5V
                MAKE_BASE=TRUE
                └── PP2V5_S3                   52

52 PP2V5_S3_VPP ═══ PP2V5_S3_VPP               107
                    MIN_LINE_WIDTH=0.1200
                    MIN_NECK_WIDTH=0.0750
                    VOLTAGE=2.5V
                    MAKE_BASE=TRUE
                    ├── PP2V5_S3_VPP           23
                    ├── PP2V5_S3_VPP           24
                    ├── PP2V5_S3_VPP           23 50
                    ├── PP2V5_S3_VPP           24
                    └── PP2V5_S3_VPP           47
```

VTT Rails

```
67 PPDDRVTT_S0_MEM ═══ PPDDRVTT_S0_MEM         106 107
                       MIN_LINE_WIDTH=0.1200
                       MIN_NECK_WIDTH=0.0750
                       VOLTAGE=1.2V
                       MAKE_BASE=TRUE
                       ├── PPDDRVTT_S0_MEM     23
                       └── PPDDRVTT_S0_MEM     24
```

Digital Ground

```
GND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0V
```

1V8 G3S Rails

```
69 PP1V8_G3S ═══ PP1V8_G3S                    59 106
                 MIN_LINE_WIDTH=0.1200
                 MIN_NECK_WIDTH=0.0750
                 VOLTAGE=1.8V
                 MAKE_BASE=TRUE
                 ├── PP1V8_G3S                34 35 107
                 ├── PP1V8_G3S                47 57
                 ├── PP1V8_G3S                68
                 ├── PP1V8_G3S                60
                 └── PP1V8_G3S                49
```

1V8 S5 Rails

```
69 PP1V8_S5 ═══ PP1V8_S5                      106
                MIN_LINE_WIDTH=0.1200
                MIN_NECK_WIDTH=0.0750
                VOLTAGE=1.8V
                MAKE_BASE=TRUE
                ├── PP1V8_S5                   47
                ├── PP1V8_S5                   12 13 15 16 17 50
                ├── PP1V8_S5                   12 16 17 38
                ├── PP1V8_S5                   16
                ├── PP1V8_S5                   13 16 17
                ├── PP1V8_S5                   18
                ├── PP1V8_S5                   35 50 71
                ├── PP1V8_S5                   45
                ├── PP1V8_S5                   16 17
                ├── PP1V8_S5                   15 72
                ├── PP1V8_S5                   90 91
                ├── PP1V8_S5                   55
                ├── PP1V8_S5                   55
                ├── PP1V8_S5                   47 63 67 73
                ├── PP1V8_S5                   20
                ├── PP1V8_S5                   113
                ├── PP1V8_S5                   45
                └── PP1V8_S5                   45
```

5V G3S Rails

```
68 PP5V_G3S ═══ PP5V_G3S                      87 106
                MIN_LINE_WIDTH=0.1200
                MIN_NECK_WIDTH=0.0750
                VOLTAGE=5V
                MAKE_BASE=TRUE
                ├── PP5V_G3S                   56
                ├── PP5V_G3S                   56
                ├── PP5V_G3S                   88
                ├── PP5V_G3S                   63
                ├── PP5V_G3S                   64 65 66 73
                ├── PP5V_G3S                   67
                ├── PP5V_G3S                   113
                ├── PP5V_G3S                   104 105
                └── PP5V_G3S                   100
```

Modified for HDMI

USBC 5V Rails

```
56 PP5V_G3S_USBC ═══ PP5V_G3S_USBC            28 94 107
                     MIN_LINE_WIDTH=0.1200
                     MIN_NECK_WIDTH=0.0750
                     VOLTAGE=5V
                     MAKE_BASE=TRUE
                     ├── PP5V_G3S_USBC         29
                     ├── PP5V_G3S_USBC         30
                     ├── PP5V_G3S_USBC         95
                     ├── PP5V_G3S_USBC         96
                     └── PP5V_G3S_USBC         104
```

USBA 5V Rails

```
56 PP5V_G3S_USBA ═══ PP5V_G3S_USBA            107
                     MIN_LINE_WIDTH=0.1200
                     MIN_NECK_WIDTH=0.0750
                     VOLTAGE=5V
                     MAKE_BASE=TRUE
                     └── PP5V_G3S_USBA         62
```

3V3 G3S Rails

```
72 PP3V3_G3S ═══ PP3V3_G3S                    59 86 106
                 MIN_LINE_WIDTH=0.1200
                 MIN_NECK_WIDTH=0.0750
                 VOLTAGE=3.3V
                 MAKE_BASE=TRUE
                 ├── PP3V3_G3S                56
                 ├── PP3V3_G3S                54
                 ├── PP3V3_G3S                51
                 ├── PP3V3_G3S                52
                 ├── PP3V3_G3S                52 53 54 56
                 └── PP3V3_G3S                51 56
```

Sensor Rails

3V3 G3S Harpoon Rails

```
56 PP3V3_G3S_WLANBT ═══ PP3V3_G3S_WLANBT
                        MIN_LINE_WIDTH=0.1010
                        MIN_NECK_WIDTH=0.0650
                        VOLTAGE=3.3V
                        MAKE_BASE=TRUE
                        ├── PP3V3_G3S_WLANBT   35 107
                        └── PP3V3_G3S_WLANBT   34
```

3V3 S5 Rails

```
70 PP3V3_S5 ═══ PP3V3_S5                      82 106
                MIN_LINE_WIDTH=0.1200
                MIN_NECK_WIDTH=0.0750
                VOLTAGE=3.3V
                MAKE_BASE=TRUE
                ├── PP3V3_S5                   16 17 20
                ├── PP3V3_S5                   12 16 17 71
                ├── PP3V3_S5                   15 16 17
                ├── PP3V3_S5                   14 16 17
                ├── PP3V3_S5                   13 15 16 17
                ├── PP3V3_S5                   12 15 16 17
                ├── PP3V3_S5                   72
                ├── PP3V3_S5                   45
                ├── PP3V3_S5                   72
                ├── PP3V3_S5                   88 90
                ├── PP3V3_S5                   20
                ├── PP3V3_S5                   21
                ├── PP3V3_S5                   113
```

GPPD is 1V8?

HDMI only 32mA?

TBT 3V3 Rails

```
54 PP3V3_S0_TBT ═══ PP3V3_S0_TBT               107
                    MIN_LINE_WIDTH=0.1200
                    MIN_NECK_WIDTH=0.0750
                    MAKE_BASE=TRUE
                    VOLTAGE=3.3V
                    ├── PP3V3_S0_TBT           72
                    └── PP3V3_S0_TBT           72
```

TBT X 3V3 Rails

```
72 PP3V3_S0SW_TBT_X ═══ PP3V3_S0SW_TBT_X       106
                        MIN_LINE_WIDTH=0.1200
                        MIN_NECK_WIDTH=0.0750
                        MAKE_BASE=TRUE
                        VOLTAGE=3.3V
                        └── PP3V3_S0SW_TBT_X   27
```

TBT T 3V3 Rails

```
72 PP3V3_S0SW_TBT_T ═══ PP3V3_S0SW_TBT_T
                        MIN_LINE_WIDTH=0.1010
                        MIN_NECK_WIDTH=0.0650
                        MAKE_BASE=TRUE
                        VOLTAGE=3.3V
                        └── PP3V3_S0SW_TBT_T   93
```

VCCSTG From Calpe HIO_SW

```
70 PP1V_S0SW ═══ PP1V_S0SW                    106
                 MIN_LINE_WIDTH=0.1200
                 MIN_NECK_WIDTH=0.0750
                 VOLTAGE=1.0V
                 MAKE_BASE=TRUE
                 └── PP1V_S0SW                 6 8 11 18
```

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: Power Aliases - 2

Apple Inc.

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BRANCH: dvt-1

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Misc Alias

71	NC_GPU_THRMTRIP	NC_GPU_THRMTRIP	MAKE_BASE=TRUE
48 30 29 28	I2C_UPC_X_SDA2	I2C_UPC_X_SDA2	MAKE_BASE=TRUE
48 30 29 28	I2C_UPC_X_SCL2	I2C_UPC_X_SCL2	MAKE_BASE=TRUE
96 95 94 48	I2C_UPC_T_SDA2	I2C_UPC_T_SDA2	MAKE_BASE=TRUE
96 95 94 48	I2C_UPC_T_SCL2	I2C_UPC_T_SCL2	MAKE_BASE=TRUE

TOP Side

105 104 102 PPBUS_HS_CPU

CC203	CC202	CC201	CC200
12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

CC231	CC230	CC229	CC228	CC227	CC226	CC225	CC224
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

77 78 75 74 112 106 105 79 76 PP1V8_SSD0

CC205	CC204
12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

105 104 102 PP12V_G3H_VIN_P5V_G3S

CC2A5	CC2A4
12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

102 PP3V3_G3H_SSD

CC207	CC206
12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

106 104 87 83 PP0V85_ENET

CC289	CC288
12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

104 102 PP12V_G3H_ACDC

CC215	CC214	CC213	CC212
12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

104 102 PP12V_MAIN

CC223	CC222	CC221	CC220	CC219	CC218	CC217	CC216
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

105 104 102 PPVCC_S0_CPU_REG

CC235	CC234	CC233	CC232	CC247	CC246	CC245	CC244
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

CC243	CC242	CC241	CC240	CC239	CC238	CC237	CC236
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

104 102 PPVCCGT_S0_CPU_REG

CC262	CC257	CC256	CC255	CC254	CC250	CC249	CC248
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

CC263	CC261	CC260	CC259	CC258	CC253	CC252	CC251
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

102 PP1V8_AWAKE

CC269	CC268	CC267	CC266	CC265	CC264
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

CC275	CC274	CC273	CC272	CC271	CC270
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

102 PP3V3_ENET

CC281	CC280	CC279	CC278	CC277	CC276
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

102 PPVIN_ENET_P0V85

CC287	CC286	CC285	CC284	CC283	CC282
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

103 PP5V_G3S_USBC

CC297	CC296	CC295	CC294	CC293	CC292	CC291	CC290
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

105 102 PP12V_G3H_VIN_P3V3_G3H

CC2A3	CC2A2	CC2A1	CC2A0	CC299	CC298
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

BOTTOM Side

105 102 PPVCCIO_S0_CPU

CC2A7	CC2A6
12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

104 102 105 PPBUS_HS_CPU

CC2B3	CC2B2	CC2B1	CC2B0	CC2A9	CC2A8
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

104 102 PPVCCGT_S0_CPU_REG

CC2B7	CC2B6	CC2B5	CC2B4
12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

104 102 105 PPVCC_S0_CPU_REG

CC2C3	CC2C2	CC2C1	CC2C0	CC2B9	CC2B8
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

103 PP1V_PRIM

CC2C9	CC2C8	CC2C7	CC2C6	CC2C5	CC2C4
12PF	3.0PF	12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

CC2D3	CC2D2	CC2D1	CC2D0
12PF	3.0PF	12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201	5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

104 102 PP12V_G3H_ACDC

CC2D5	CC2D4
12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

104 102 PP12V_MAIN

CC2D7	CC2D6
12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

104 87 83 106 PP0V85_ENET

CC2D8	CC2D9
12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

105 103 PP5V_G3S

CC2E0	CC2E1
12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

105 104 102 PP12V_G3H_VIN_P5V_G3S

CC2E3	CC2E2
12PF	3.0PF
5% 25V NP0-C0G 0201	+/-0.1PF 25V NP0-C0G 0201

BOM_COST_GROUP=DESENSE

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Apple Inc.

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8	7	6	5	4	3	2	1

PPVDDCPU_AWAKE_SOC
- CC303 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC302 2.7PF +/-0.1PF 25V C0G-CERM 0201 CRITICAL NOSTUFF

PP1V1_SLPDDR
- CC331 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC332 2.7PF +/-0.1PF 25V C0G-CERM 0201 CRITICAL NOSTUFF

PP1V8_SSD0
PLACE_NEAR=U8600.P9:3MM PLACE_NEAR=U8700.P9:3MM PLACE_NEAR=U8800.P9:3MM PLACE_NEAR=U8900.P9:3MM
PLACE_NEAR=U8600.T5:3MM PLACE_NEAR=U8700.T5:3MM PLACE_NEAR=U8800.T5:3MM PLACE_NEAR=U8900.T5:3MM
- CC323 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC322 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC321 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC320 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC319 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC318 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC317 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC316 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PPVCCIO_S0_CPU_REG
- CC3B7 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3B6 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3B5 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3B4 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP0V82_SLPDDR
- CC301 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC300 2.7PF +/-0.1PF 25V C0G-CERM 0201 CRITICAL NOSTUFF

PP0V9_SLPDDR
PLACE_NEAR=C4410:3MM
- CC329 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC328 2.7PF +/-0.1PF 25V C0G-CERM 0201 CRITICAL NOSTUFF
PLACE_NEAR=C4411:3MM NOSTUFF

PP2V7_NAND_SSD0
PLACE_NEAR=U8600.R2:3MM PLACE_NEAR=U8700.R2:3MM PLACE_NEAR=U8800.R2:3MM PLACE_NEAR=U8900.R2:3MM
PLACE_NEAR=U8600.G4:3MM PLACE_NEAR=U8700.G4:3MM PLACE_NEAR=U8800.G4:3MM PLACE_NEAR=U8900.G4:3MM
- CC397 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC396 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC395 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC394 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC393 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC392 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC391 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC390 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP12V_G3H_VIN_P5V_G3S
- CC349 12PF 5% 50V C0G-CERM 0201 CRITICAL NOSTUFF
- CC348 3PF +/-0.1PF 100V C0G 0201 CRITICAL NOSTUFF
- CC3A9 12PF 5% 50V C0G-CERM 0201 CRITICAL NOSTUFF
- CC3A8 3PF +/-0.1PF 100V C0G 0201 CRITICAL NOSTUFF

PP1V8_SSD0_S4E0_AVDD18_PLL
PLACE_NEAR=U8600.L2:3MM
- CC305 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC304 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP1V8_SSD0_S4E1_AVDD18_PLL
PLACE_NEAR=U8700.L2:3MM
- CC3A5 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3A4 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP1V8_SSD0_S4E2_AVDD18_PLL
PLACE_NEAR=U8800.L2:3MM
- CC307 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC306 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP1V8_SSD0_S4E3_AVDD18_PLL
PLACE_NEAR=U8900.L2:3MM
- CC389 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC388 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP0V9_SSD0
PLACE_NEAR=U8600.R4:3MM PLACE_NEAR=U8600.R8:3MM PLACE_NEAR=U8600.J8:3MM
PLACE_NEAR=U8600.G8:3MM
- CC369 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC368 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC367 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC366 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC365 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC364 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP1V2_S3
- CC3D3 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3D2 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3D1 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3D0 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP5V_G3S
- CC3C1 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3C0 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3B9 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3B8 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP1V8_SSD0_S4E0_PCI_AVDD_H
PLACE_NEAR=U8600.J6:3MM
- CC335 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC334 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP1V8_SSD0_S4E1_PCI_AVDD_H
PLACE_NEAR=U8700.J6:3MM
- CC333 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC308 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP1V8_SSD0_S4E2_PCI_AVDD_H
PLACE_NEAR=U8800.J6:3MM
- CC347 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC346 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP1V8_SSD0_S4E3_PCI_AVDD_H
PLACE_NEAR=U8900.J6:3MM
- CC345 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC344 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP0V9_SSD0
PLACE_NEAR=U8700.R4:3MM PLACE_NEAR=U8700.R8:3MM PLACE_NEAR=U8700.J8:3MM
PLACE_NEAR=U8700.G8:3MM
- CC375 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC374 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC373 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC372 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC371 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC370 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP3V3_G3H
PLACE_NEAR=L7610:3MM PLACE_NEAR=L7610:3MM
- CC3C9 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3C8 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3C7 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3C6 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3C5 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3C4 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PLACE_NEAR=L7610:3MM PLACE_NEAR=L7610:3MM PLACE_NEAR=L7610:3MM PLACE_NEAR=L7610:3MM NOSTUFF

PP0V9_SSD0
PLACE_NEAR=U8800.R4:3MM PLACE_NEAR=U8800.R8:3MM PLACE_NEAR=U8800.J8:3MM
PLACE_NEAR=U8800.G8:3MM
- CC3A3 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3A2 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3A1 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3A0 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC399 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC398 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP0V9_SSD0
PLACE_NEAR=U8900.R4:3MM PLACE_NEAR=U8900.R8:3MM PLACE_NEAR=U8900.J8:3MM
PLACE_NEAR=U8900.G8:3MM PLACE_NEAR=U8900.J6:3MM
- CC381 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC380 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC379 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC378 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC377 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC376 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP3V3_G3H_SSD
PLACE_NEAR=U9000.B4:3MM
PLACE_NEAR=U9000.B4:3MM
- CC315 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC314 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP0V9_SSD0
PLACE_NEAR=C9025:3MM
- CC313 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC312 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
PLACE_NEAR=C9025:3MM NOSTUFF

PP1V8_SSD0
PLACE_NEAR=C9035:3MM
- CC327 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC326 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF
PLACE_NEAR=C9035:3MM NOSTUFF

PPBUS_HS_CPU
PLACE_NEAR=R5420:3MM
- CC354 12PF 5% 50V C0G-CERM 0201 CRITICAL NOSTUFF
- CC350 3PF +/-0.1PF 100V C0G 0201 CRITICAL
PLACE_NEAR=R5420:3MM NOSTUFF

PPVCC_S0_CPU_REG
- CC3C3 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3C2 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP12V_G3H_VIN_P3V3_G3H
PLACE_NEAR=R5420:3MM
- CC3B3 12PF 5% 50V C0G-CERM 0201 CRITICAL NOSTUFF
- CC3B2 3PF +/-0.1PF 100V C0G 0201 CRITICAL
PLACE_NEAR=R5420:3MM NOSTUFF

PP3V3_ENET
PLACE_NEAR=U9300.14:3MM
PLACE_NEAR=U9300.14:3MM
- CC343 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC342 2.7PF +/-0.1PF 25V C0G-CERM 0201 CRITICAL NOSTUFF

ENET_XTALVDDH
PLACE_NEAR=U9300.17:3MM
PLACE_NEAR=U9300.17:3MM
- CC341 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC340 2.7PF +/-0.1PF 25V C0G-CERM 0201 CRITICAL NOSTUFF

PPHV_USBC_XA
PLACE_NEAR=U3100:3MM
- CC3E1 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3E2 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL
PLACE_NEAR=U3100:3MM NOSTUFF

PPHV_USBC_XB
PLACE_NEAR=U3200:3MM
- CC3D8 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3D7 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL
PLACE_NEAR=U3200:3MM NOSTUFF

PP3V3_ENET_PHY_BIASVDDH
PLACE_NEAR=U9300.37:3MM
PLACE_NEAR=U9300.37:3MM
- CC339 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC338 2.7PF +/-0.1PF 25V C0G-CERM 0201 CRITICAL NOSTUFF

PP3V3_ENET_PHY_AVDDH
PLACE_NEAR=U9300.42:3MM
PLACE_NEAR=U9300.42:3MM
- CC337 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC336 2.7PF +/-0.1PF 25V C0G-CERM 0201 CRITICAL NOSTUFF

PPHV_USBC_TA
PLACE_NEAR=UB300:3MM
- CC310 12PF 5% 50V C0G-CERM 0201 CRITICAL NOSTUFF
- CC309 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL
PLACE_NEAR=UB300:3MM NOSTUFF

PPHV_USBC_TB
PLACE_NEAR=UB400:3MM
- CC3D6 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC311 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL
PLACE_NEAR=UB400:3MM NOSTUFF

PP1V2_ENET_INTREG
PLACE_NEAR=U9300.13:3MM
PLACE_NEAR=U9300.13:3MM
- CC325 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC324 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP1V2_ENET_PHY_AVDDL
PLACE_NEAR=U9300.45:3MM
PLACE_NEAR=U9300.45:3MM
- CC387 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC386 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP12V_MAIN
- CC362 12PF 5% 50V C0G-CERM 0201 CRITICAL NOSTUFF
- CC357 3PF +/-0.1PF 100V C0G 0201 CRITICAL NOSTUFF
- CC356 12PF 5% 50V C0G-CERM 0201 CRITICAL NOSTUFF
- CC355 3PF +/-0.1PF 100V C0G 0201 CRITICAL NOSTUFF

PPVCCIO_S0_CPU
- CC3A7 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC3A6 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP1V2_ENET_PHY_PCIEPLL
PLACE_NEAR=U9300.29:3MM
PLACE_NEAR=U9300.29:3MM
- CC385 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC384 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP1V2_ENET_PHY_GPHYPLL
PLACE_NEAR=U9300.36:3MM
PLACE_NEAR=U9300.36:3MM
- CC383 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC382 3.0PF +/-0.1PF 25V NP0-C0G 0201 CRITICAL NOSTUFF

PP12V_S0_CPUCORE_FLT
- CC363 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC361 3PF +/-0.1PF 100V C0G 0201 CRITICAL NOSTUFF
- CC360 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC359 3PF +/-0.1PF 100V C0G 0201 CRITICAL NOSTUFF
- CC358 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC353 3PF +/-0.1PF 100V C0G 0201 CRITICAL NOSTUFF
- CC352 12PF 5% 25V NP0-C0G 0201 CRITICAL NOSTUFF
- CC351 3PF +/-0.1PF 100V C0G 0201 CRITICAL NOSTUFF

BOM_COST_GROUP=DESENSE

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DFU AND FCT TESTPOINTS placed on top side of MLB, oppsite from CPU.

DFU TEST POINTS <RDAR://31619312>

Possibly useful panda signals

removed SOC_DEBUGPRT_RX/TX

TPC402	1 TP-P5	DEBUG_JTAG_SOC_TDO	38 113
TPC403	1 TP-P5	DEBUG_JTAG_SOC_TDI	38 113
TPC404	1 TP-P5	PP1V8_SLPS2R	84 102
TPC405	1 TP-P5	SOC_SOCHOT_L	37 71 113
TPC406	1 TP-P5	I2C_PWR_SDA	38 48
TPC407	1 TP-P5	I2C_UPC_SCL	38 48
TPC4E9	1 TP-P5	I2C_UPC_SDA	38 48
TPC4F0	1 TP-P5	DFUMUX_SEL	113
TPC4Z5	1 TP-P5	I2C_PWR_SCL	38 48
TPC401	1 TP-P5	USB_SOC_P	37 113
TPC431	1 TP-P5	USB_SOC_N	37 113
TPC440	1 TP-P5		
TPC439	1 TP-P5		
TPC4G6	1 TP-P5		

Other I2C TPs

Possibly useful panda signals

TPC435	1 TP-P5	I2C_FAN_SCL	48 57
TPC438	1 TP-P5	I2C_FAN_SDA	48 57

DFU NON-CUSTOMER-FACING USB PORTS

PLACE IN ACCESSIBLE BOARD AREA

SWDL

TPC408	1 TP-P5	USB3_TEST_D2R_N	OUT 14
TPC409	1 TP-P5	USB3_TEST_D2R_P	OUT 14
TPC410	1 TP-P5	USB3_TEST_R2D_N	IN 14
TPC411	1 TP-P5	USB3_TEST_R2D_P	IN 14
TPC412	1 TP-P5		
TPC413	1 TP-P5		
TPC414	1 TP-P5		
TPC415	1 TP-P5		
TPC416	1 TP-P5	USB_TEST_N	BI 14
TPC417	1 TP-P5	USB_TEST_P	BI 14
TPC418	1 TP-P5		

DZC400 5.5V-0.28PF 0201-THICKSTNCL; DZC401 5.5V-0.28PF 0201-THICKSTNCL; DZC402 5.5V-0.28PF 0201-THICKSTNCL; DZC403 5.5V-0.28PF 0201-THICKSTNCL; DZC408 5.5V-0.28PF 0201-THICKSTNCL; DZC409 5.5V-0.28PF 0201-THICKSTNCL

NON-CUSTOMER-FACING USB PORTS FOR ETHERNET DONGLE(Bristol OS Testing)

PLACE IN ACCESSIBLE BOARD AREA

Ethenet

TPC422	1 TP-P5	USB3_ENET_ADAPTOR_D2R_N	OUT 14
TPC423	1 TP-P5	USB3_ENET_ADAPTOR_D2R_P	OUT 14
TPC424	1 TP-P5	USB3_ENET_ADAPTOR_R2D_N	IN 14
TPC425	1 TP-P5	USB3_ENET_ADAPTOR_R2D_P	IN 14
TPC426	1 TP-P5		
TPC427	1 TP-P5		
TPC428	1 TP-P5		
TPC429	1 TP-P5		
TPC419	1 TP-P5	USB_ENET_ADAPTOR_N	BI 14
TPC420	1 TP-P5	USB_ENET_ADAPTOR_P	BI 14
TPC421	1 TP-P5		
TPC430	1 TP-P5	PP5V_G3S	87 103 106

DZC410 5.5V-0.28PF 0201-THICKSTNCL; DZC411 5.5V-0.28PF 0201-THICKSTNCL; DZC412 5.5V-0.28PF 0201-THICKSTNCL; DZC413 5.5V-0.28PF 0201-THICKSTNCL; DZC406 5.5V-0.28PF 0201-THICKSTNCL; DZC407 5.5V-0.28PF 0201-THICKSTNCL

AUDIO JACK

107 61	IN	AUD_CONN_HP_LEFT	
107 61	IN	AUD_CONN_HP_RIGHT	
107 61	IN	AUD_CONN_RING2	
107 61	IN	AUD_CONN_SLEEVE	
107 61	IN	AUD_CONN_HP_SENSE_L	
107 61	IN	AUD_CONN_HP_SENSE_R	
107 61	IN	AUD_CONN_TIP_SENSE	
107 61	IN	AUD_CONN_SLEEVE_XW	
107 61	IN	AUD_CONN_RING2_XW	
TPC4Z9	1 TP-P5	GND_AUDIO_CODEC	59

DEBUG MOJO

TPC451	1 TP-P5	PCH_UART_DEBUG_R2D	15 28 113
TPC452	1 TP-P5	PCH_UART_DEBUG_D2R	15 28 113

removed SMC_DEBUGPRT_RX/TX

TPC453	1 TP-P5		

Soc Access w/o Potassium

TPC454	1 TP-P5	SOC_USB_VBUS	28 37 113
TPC455	1 TP-P5	USB_SOC_TYPEC_P	28 113
TPC456	1 TP-P5	USB_SOC_TYPEC_N	28 113
TPC457	1 TP-P5	PMU_ACTIVE_READY	29 37 71 108 110
TPC458	1 TP-P5	SOC_FORCE_DFU	28 37 71 113
TPC459	1 TP-P5	SOC_DFU_STATUS	28 37
TPC460	1 TP-P5	UPC_XB_DBG3	28 30
TPC461	1 TP-P5	UPC_XB_DBG4	28 30
TPC462	1 TP-P5	SOC_DOCK_CONNECT	29 30 38
TPC463	1 TP-P5	SOC_SWD_MUX_SEL_PCH	15
TPC464	1 TP-P5		

Power Sequence,status,charging

TPC468	1 TP-P5	PP12V_MAIN	102 105
TPC469	1 TP-P5	PP1V2_S3	103 107
TPC470	1 TP-P5	PPVCC_S0_CPU_REG	102
TPC471	1 TP-P5	PP5V_G3S	87 103 106
TPC472	1 TP-P5	PMU_ONOFF_L	71 100
TPC4L6	1 TP-P5	CPU_PWRGD	6 13 108
TPC474	1 TP-P5	PMU_ONOFF_R_L	100 113
TPC475	1 TP-P5	PM_SLP_S3_L	12 14 25 80 92 106 110
TPC476	1 TP-P5	PM_SLP_S4_L	12
TPC477	1 TP-P5	PM_SLP_S5_L	12 110
TPC478	1 TP-P5	PM_RSMRST_L	12 18 45 47 88 106 110
TPC479	1 TP-P5	PPDDRVTT_S0_MEM	103 107
TPC481	1 TP-P5	PP1V_S3	103
TPC482	1 TP-P5	PM_SYSRST_L	12 18 45 108
TPC483	1 TP-P5	PM_PCH_SYS_PWROK	12 45
TPC484	1 TP-P5	PM_PCH_PWROK	12 34 45 108
TPC485	1 TP-P5	PLT_RST_L	12 13 15 20 110
TPC487	1 TP-P5	PM_SLP_S0_L	12 38 71 100
TPC488	1 TP-P5	SMC_FIXTURE_MODE_L	38
TPC489	1 TP-P5	PP1V8_G3S	59 103
TPC490	1 TP-P5	PP5V_G3S	87 103 106
TPC491	1 TP-P5	PP3V3_G3H	102 105
TPC492	1 TP-P5	PP3V3_G3H_SSD	102
TPC493	1 TP-P5	PP3V3_S0SW_TBT_X	103
TPC4B4	1 TP-P5	PPVDDCPU_AWAKE_SOC	102
TPC4B6	1 TP-P5	PVDDQ_EN	47 71
TPC4B7	1 TP-P5	PVCCIO_EN	71 73
TPC4B8	1 TP-P5	PP0V9_SLPDDR	102
TPC4B9	1 TP-P5	PP1V1_SLPDDR	102
TPC4C0	1 TP-P5	PP1V1_SLPS2R	102
TPC4C1	1 TP-P5	PP1V8_AWAKE	102
TPC4J1	1 TP-P5	SMC_SYSRST_L	38 45 108
TPC4C4	1 TP-P5	PP1V8_SLPS2R_PMUVDDGPIO	69
TPC4C5	1 TP-P5	P1V1_SLPDDR_SOCFET_EN	70 71
TPC4C6	1 TP-P5	PMU_CLK32K_WLANBT_R	35 71
TPC4C7	1 TP-P5	SOC_WDOG	38 71
TPC4C8	1 TP-P5	PMU_CLK32K_SOC	38 71
TPC4C9	1 TP-P5	PMU_SYS_ALIVE	37 38 71 79 88
TPC437	1 TP-P5		

BOM_COST_GROUP=DEBUG

Power Sequence,status,charging

TPC4D0	1 TP-P5	P5VG3S_EN	47 71 100
TPC4D1	1 TP-P5	PP0V8_SLPS2R	102
TPC4D2	1 TP-P5	PPVDDCPUSRAM_AWAKE	102
TPC4D3	1 TP-P5	P5VG3S_PGOOD	47 71
TPC4D4	1 TP-P5	CPUVR_PGOOD	47 71 110
TPC4L7	1 TP-P5	PPVCCGT_S0_CPU_REG	102
TPC4F3	1 TP-P5	PPVCCSA_S0_CPU_REG	102
TPC4L0	1 TP-P5	PPVCCIO_S0_CPU	102
TPC4F4	1 TP-P5	PP1V_S0SW	103
TPC4F5	1 TP-P5	PP1V2_S0SW	103
TPC4F6	1 TP-P5	PP1V_PRIM	103
TPC4F7	1 TP-P5	PP1V8_S5	103
TPC4F8	1 TP-P5	PP3V0_G3H_RTC	102
TPC4F9	1 TP-P5	ALL_SYS_PWRGD	45 71 110
TPC4G0	1 TP-P5	PCH_RTC_RESET_L	12 71
TPC4G1	1 TP-P5	PM_THRMTRIP_L	13 20
TPC4G2	1 TP-P5	PM_PWRBTN_L	12 20
TPC4G3	1 TP-P5	CPU_PROCHOT_R_L	6
TPC4G4	1 TP-P5	PP1V2_ENET	83 86
TPC4I2	1 TP-P5	PP0V85_ENET	83 87 104
TPC4G7	1 TP-P5	PP2V1_ENET	83 86
TPC4G8	1 TP-P5	PP3V3_G3H_ENET	85 102
TPC4G9	1 TP-P5	PP3V3_AWAKE	102
TPC4H0	1 TP-P5	PMU_COLD_RESET_L	38 71 108
TPC4H1	1 TP-P5	PP0V82_SLPDDR	102
TPC4H3	1 TP-P5	PMU_PVDDMAIN_EN	68 71
TPC4H4	1 TP-P5	UPC_PMU_RESET	28 71
TPC4H5	1 TP-P5	P3V3G3S_EN	47 71
TPC4H6	1 TP-P5	PP3V3_G3S	59 86 103
TPC4H7	1 TP-P5	TP_P1V8G3S_EN	71
TPC4L1	1 TP-P5	SSD_PMU_RESET_L	37 46 79
TPC4L2	1 TP-P5	PP2V7_NAND_SSD0	75 76 77 78 79 105 112
TPC4I0	1 TP-P5	PP3V3_S5	82 103
TPC4I1	1 TP-P5	PP0V9_SSD0	75 76 77 78 79 105 112
TPC4I4	1 TP-P5	PP1V8_SSD0	112
TPC4I5	1 TP-P5	PP1V2_AWAKE	112 74 75 76 77 78 79 104 105 102

Soc Access with Potassium

TPC436	1 TP-P5	USBC_XB_SBU1	30 31
TPC4A0	1 TP-P5	USBC_XB_SBU2	30 31
TPC400	1 TP-P5	USBC_XA_CC1	29 31
TPC4A2	1 TP-P5	PPVBUS_USBC_XA	28, 29 31 107
TPC4A3	1 TP-P5		

ACDC Power Input TPs

TPC4A4	1 TP-P5	PP12V_G3H_ACDC	102 106
TPC4A5	1 TP-P5	PP12V_G3H_ACDC	102 106
TPC4A6	1 TP-P5	PP12V_G3H_ACDC	102 106
TPC4A7	1 TP-P5	PP12V_G3H_ACDC	102 106
TPC4A8	1 TP-P5	PP12V_G3H_ACDC	102 106
TPC4A9	1 TP-P5	PP12V_G3H_ACDC	102 106
TPC4B1	1 TP-P5		
TPC4B2	1 TP-P5		
TPC4B3	1 TP-P5		
TPC4C2	1 TP-P5		
TPC4D5	1 TP-P5		
TPC4D6	1 TP-P5		
TPC434	1 TP-P5	PP12V_G3H_ACDC	102 106
TPC432	1 TP-P5	PP12V_G3H_ACDC	102 106
TPC433	1 TP-P5	PP12V_G3H_ACDC	102 106

PAGE TITLE

DFU TEST POINTS

Apple Inc.

DRAWING NUMBER 051-02424 SIZE D

REVISION 6.0.0

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FCT TEST POINTS (TOP SIDE OF MLB)

AUDIO

TPC597	A	1	TP-P5	
TPC5A1	A	1	TP-P5	SPKRCONN_OUTP
TPC5A0	A	1	TP-P5	SPKRCONN_OUTN
TPC598	A	1	TP-P5	
TPC510	A	1	TP-P5	SPKRCONN_OUTP
TPC511	A	1	TP-P5	SPKRCONN_OUTN
TPC5A2	A	1	TP-P5	
TPC5B8	A	1	TP-P5	AUD_CONN_RING_SENSE
TPC5B7	A	1	TP-P5	AUD_CONN_RING2_XW
TPC5B6	A	1	TP-P5	AUD_CONN_TIP_SENSE
TPC5B5	A	1	TP-P5	AUD_CONN_HP_SENSE_R
TPC5A7	A	1	TP-P5	
TPC5B3	A	1	TP-P5	AUD_CONN_HP_SENSE_L
TPC5A8	A	1	TP-P5	AUD_CONN_HP_LEFT
TPC5A9	A	1	TP-P5	AUD_CONN_HP_RIGHT
TPC5B0	A	1	TP-P5	AUD_CONN_RING2
TPC5B2	A	1	TP-P5	AUD_CONN_SLEEVE
TPC5K0	A	1	TP-P5	
TPC5K1	A	1	TP-P5	AUD_CONN_SLEEVE_XW

HDMI Test Poins

TPC556	A	1	TP-P5	HDMI_CEC_CONN
TPC557	A	1	TP-P5	HDMI_RSVD
TPC561	A	1	TP-P5	HDMI_DDC_5V_CONN_SCL
TPC563	A	1	TP-P5	HDMI_DDC_5V_CONN_SDA
TPC5Y9	A	1	TP-P5	HDMI_HPD_IN_CONN
TPC592	A	1	TP-P5	PP5V0_HDMI_DDC_CONN
TPC593	A	1	TP-P5	
TPC594	A	1	TP-P5	

USBC (PLACE NEAR CONNECTOR)

TPC5G4	A	1	TP-P5	USBC_XA_SBU1
TPC5G5	A	1	TP-P5	USBC_XA_SBU2
TPC5G6	A	1	TP-P5	USBC_TA_SBU1
TPC507	A	1	TP-P5	USBC_TA_SBU2
TPC508	A	1	TP-P5	USBC_TB_SBU1
TPC509	A	1	TP-P5	USBC_TB_SBU2
TPC5G7	A	1	TP-P5	USBC_XA_CC2
TPC5G9	A	1	TP-P5	PPVBUS_USBC_XA
TPC5H0	A	1	TP-P5	PPVBUS_USBC_XA
TPC5H1	A	1	TP-P5	PPVBUS_USBC_XA
TPC5H3	A	1	TP-P5	PPVBUS_USBC_XB
TPC5H4	A	1	TP-P5	PPVBUS_USBC_XB
TPC5I8	A	1	TP-P5	PPVBUS_USBC_XB
TPC5J1	A	1	TP-P5	PPVBUS_USBC_TA
TPC5J0	A	1	TP-P5	PPVBUS_USBC_TA
TPC5J2	A	1	TP-P5	PPVBUS_USBC_TA
TPC5J4	A	1	TP-P5	PPVBUS_USBC_TB
TPC5H5	A	1	TP-P5	PPVBUS_USBC_TB
TPC5H6	A	1	TP-P5	PPVBUS_USBC_TB
TPC5H7	A	1	TP-P5	
TPC5H8	A	1	TP-P5	
TPC5M2	A	1	TP-P5	
TPC5K2	A	1	TP-P5	
TPC5K3	A	1	TP-P5	
TPC5K4	A	1	TP-P5	
TPC5J5	A	1	TP-P5	
TPC5J6	A	1	TP-P5	
TPC5N9	A	1	TP-P5	USBC_XB_CC1
TPC5N8	A	1	TP-P5	USBC_XB_CC2
TPC5O1	A	1	TP-P5	USBC_TA_CC1
TPC5O2	A	1	TP-P5	USBC_TA_CC2
TPC5O3	A	1	TP-P5	USBC_TB_CC1
TPC5O4	A	1	TP-P5	USBC_TB_CC2

FAN Test Points

TPC558	A	1	TP-P5	FAN_0_PWM_FILT
TPC559	A	1	TP-P5	FAN_0_TACH_FILT
TPC562	A	1	TP-P5	PP12V_FAN_FILT
TPC564	A	1	TP-P5	
TPC565	A	1	TP-P5	

MISC

TPC540	A	1	TP-P5	SYS_LED_DR
TPC541	A	1	TP-P5	ISNS_P1V2_N
TPC542	A	1	TP-P5	ISNS_P1V2_P
TPC543	A	1	TP-P5	ISNS_P3V3_G3H_HI_N
TPC544	A	1	TP-P5	ISNS_P3V3_G3H_HI_P
TPC545	A	1	TP-P5	ISNS_P3V3_WLANBT_N
TPC548	A	1	TP-P5	ISNS_P3V3_WLANBT_P
TPC547	A	1	TP-P5	ISNS_P5V_G3S_HI_N
TPC546	A	1	TP-P5	ISNS_P5V_G3S_HI_P
TPC549	A	1	TP-P5	ISNS_PMU_N
TPC512	A	1	TP-P5	ISNS_PMU_P
TPC551	A	1	TP-P5	PMU_P3V3_CAPLE_ISENSE
TPC552	A	1	TP-P5	PP12V_FAN_FET
TPC513	A	1	TP-P5	PP12V_G3H_VIN_P3V3_G3H
TPC515	A	1	TP-P5	PP12V_G3H_VIN_P5V_G3S
TPC514	A	1	TP-P5	PP12V_S0_CPUCORE_FLT
TPC518	A	1	TP-P5	PP2V5_S3_VPP
TPC517	A	1	TP-P5	PP3V3_G3H_PMU
TPC516	A	1	TP-P5	PP3V3_S0_TBT
TPC519	A	1	TP-P5	PP5V_G3S_USBA
TPC523	A	1	TP-P5	PP5V_G3S_USBC
TPC522	A	1	TP-P5	PPBUS_HS_CPU
TPC520	A	1	TP-P5	PPCPUVCCSA_S0_SENSE_1
TPC521	A	1	TP-P5	PPVCCIO_S0_CPU_REG
TPC524	A	1	TP-P5	PPVDDQ_S3_REG_R
TPC527	A	1	TP-P5	PPVIN_ENET_P0V85
TPC526	A	1	TP-P5	PPVIN_G3H_P2V7
TPC525	A	1	TP-P5	SMC_CPU_HI_ISENSE
TPC528	A	1	TP-P5	SMC_CPU_VCC_ISENSE
TPC529	A	1	TP-P5	SMC_CPUGT_ISENSE
TPC530	A	1	TP-P5	SMC_P12VIN_ISENSE
TPC531	A	1	TP-P5	SMC_P1V2_ISENSE
TPC534	A	1	TP-P5	XDP_CPU_TCK
TPC533	A	1	TP-P5	XDP_CPU_TDI
TPC532	A	1	TP-P5	XDP_CPU_TDO
TPC535	A	1	TP-P5	XDP_CPU_TMS
TPC536	A	1	TP-P5	XDP_CPU_TRST_L

WIRELESS

TPC5H9	A	1	TP-P5	PP3V3_G3S_WLANBT
TPC5I0	A	1	TP-P5	PP1V8_G3S
TPC5L0	A	1	TP-P5	PPVIN_RFLDO_WLANBT
TPC5L1	A	1	TP-P5	PP1V2_WLANBT
TPC5L2	A	1	TP-P5	PP1V5_WLANBT

MEMORY

TPC5I3	A	1	TP-P5	PVDDQ_PGOOD
TPC5I4	A	1	TP-P5	PP1V2_S3
TPC5I5	A	1	TP-P5	PP2V5_S3
TPC5I6	A	1	TP-P5	PPDDRVTT_S0_MEM
TPC5I7	A	1	TP-P5	PP1V2_S3

HDMI

TPC505	A	1	TP-P5	DDI2_MUX_SEL
TPC506	A	1	TP-P5	DDI1_MUX_SEL

USB-A Test Poins

High Speed - Tear drops, NO TP

IN	USB3_EXTA_TX_F_P		
IN	USB3_EXTA_TX_F_N		
IN	USB3_EXTA_RX_P		
IN	USB3_EXTA_RX_N		
IN	USB2_EXTA_P		
IN	USB2_EXTA_N		
IN	USB3_EXTB_TX_F_P		
IN	USB3_EXTB_TX_F_N		
IN	USB3_EXTB_RX_P		
IN	USB3_EXTB_RX_N		
IN	USB2_EXTB_P		
IN	USB2_EXTB_N		

TPC595	A	1	TP-P5	PP5V_S4_EXTA_F
TPC596	A	1	TP-P5	PP5V_S4_EXTB_F
TPC599	A	1	TP-P5	
TPC5A6	A	1	TP-P5	
TPC5C5	A	1	TP-P5	PP5V_S4_EXTA_F
TPC5C6	A	1	TP-P5	PP5V_S4_EXTB_F
TPC5C7	A	1	TP-P5	
TPC5C8	A	1	TP-P5	

ENET HS signals - Tear drops, NO TP

IN	ENET_CONN_A_P	
IN	ENET_CONN_A_N	
IN	ENET_CONN_B_P	
IN	ENET_CONN_B_N	
IN	ENET_CONN_C_P	
IN	ENET_CONN_C_N	
IN	ENET_CONN_D_P	
IN	ENET_CONN_D_N	

PSU Test Points

TPC501	A	1	TP-P5	SNS_ACDC_P
TPC500	A	1	TP-P5	SNS_ACDC_N
TPC503	A	1	TP-P5	ACDC_ID
TPC504	A	1	TP-P5	ACDC_BURST_EN_L
TPC502	A	1	TP-P5	SYS_LED

BOM_COST_GROUP=PCB

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PAGE TITLE: FCT TESTPOINTS

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ICT TEST POINTS, ICT BOUNDARY SCAN TESTPOINTS

CPU XDP and PCH Test-Points

107 18 6	IN	XDP_CPU_TCK
18 13	IN	XDP_PCH_TCK
107 18 6	IN	XDP_CPU_TDI
107 18 6	IN	XDP_CPU_TDO
107 18 13 6	IN	XDP_CPU_TRST_L
107 18 6	IN	XDP_CPU_TMS
18 13	IN	XDP_PCH_TMS
18 13	IN	XDP_PCH_TDI
18 13	IN	XDP_PCH_TDO
18 13 6	IN	XDP_CPU_PREQ_L
18 13 6	IN	XDP_CPU_PRDY_L
47 45 18 13 110 106 86	IN	PM_RSMRST_L
106 45 34 12	IN	PM_PCH_PWROK
106 45 18 12	IN	PM_SYSRST_L
18 6	IN	CPU_CFG<3>
18 13	IN	PCH_JTAGX
18 13	BI	PCH_ITP_PMODE

H9M BOUNDARY SCAN TESTPOINTS ON FCT TESTPOINT PAGE

OTHER ICT TESTPONTS

ACE

26 15	BI	JTAG_TBT_X_TMS
94 92 26	BI	JTAG_ISP_TDI
94 92 26	BI	JTAG_ISP_TCK
94 92 26	BI	JTAG_ISP_TDO
108 26	BI	TBT_X_TEST_EN

WLAN

38 36	BI	WLAN_JTAG_TMS
38 36	BI	WLAN_JTAG_TCK
39 36	BI	WLAN_JTAG_TDI
36 35	BI	WLAN_JTAG_TDO
36 35	BI	WLAN_JTAG_TRST_L
92 15	BI	JTAG_TBT_T_TMS
38	BI	TP_JTAG_SOC_TRST_L
45 38	BI	SMC_PCH_SYS_PWROK
45 38	BI	SMC_PCH_PWROK
106 45 38	BI	SMC_SYSRST_L
106 13 6	BI	CPU_PWRGD
106 71 38	BI	PMU_COLD_RESET_L
38	BI	SOC_JTAG_SEL
37	BI	SOC_TESTMODE
36 35	BI	WLAN_JTAG_SEL
92	BI	TBT_T_TEST_EN
108 26	BI	TBT_X_TEST_EN

TP of HDMI (EE tests)

TPC646	DP2HDMI_PMU_CEC_IRQ	90
TPC641	DP2HDMI_1.5G_FILT_EN	88 90

TP of Calpe PMIC (EE tests)

TPC642	TP_PP1V8_PMU_BUCK3SW5	69
TPC643	TP_PP1V1_PMU_BUCK4SW1	69
TPC644	TP_PP1V2_PMU_BUCK6SW1	69 108
TPC645	TP_PP1V_PMU_BUCK8SW1	69 108
TPC676	SOC_VDDCPU_SENSE	41 71
TPC664	TP_P3V3G3W_EN	71
TPC665	TP_P3V3G3W_PGOOD	71
TPC667	TP_SE_PWR_EN	71
TPC668	TP_P3V3_S5_EN	
TPC670	TP_PVCCEOPIOEDRAM_P2V7NAND_PGOOD	
TPC671	TP_PEARL_P2V7NAND_EN	71
TPC672	TP_NAND_DISCHARGE_HDD_PWR_EN	71
TPC673	TP_NAND_RESET_L_SD_PWR_EN	71
TPC674	ENET_PWR_EN	71 72 85 86 87
TPC675	TBT_PWR_EN	71 72
TPC679	UPC_TA_GPIO7	95
TPC635	BT_PWR_EN	35 36 71
TPC669	WLAN_PWR_EN	35 36 71
TPC680	UPC_TB_GPIO7	96
TPC681	TP_PP1V2_PMU_BUCK6SW1	69 108
TPC682	TP_PP1V_PMU_BUCK8SW1	69 108
TPC677	FAN_PWR_EN	57 71
TPC683	PVCCIO_PGOOD	47 71
TPC684	P3V3MAIN_PGOOD	47 71 110
TPC636	PVCCPLLOC_EN	71 72

Test Points for Calpe breakout

TPC647	PMU_VCCIO_ISENSE	46 71 108
TPC648	PMU_VCCIO_ISENSE	46 71 108
TPC649	PMU_VCCIO_ISENSE	46 71 108
TPC650	PMU_P5V_G3S_HI_ISENSE	46 71
TPC651	PMU_CPUSA_VSENSE	46 71
TPC652	PMU_P5V_USBC_ISENSE	46 71
TPC653	PMU_P5V_USBA_ISENSE	46 71
TPC654	TP_PMU_AMUX_AY	71
TPC655	PMU_P3V3_TBT_ISENSE	46 71
TPC656	PMU_P3V3_SSD0_ISENSE	46 71
TPC657	PMU_PBUS_SSD0_ISENSE	46 71
TPC658	PMU_P3V3_G3H_HI_ISENSE	46 71
TPC659	PMU_P3V3_WLANBT_ISENSE	46 71
TPC660	PMU_P3V3_ENET_ISENSE	46 71
TPC661	PMU_P12V_ENET_ISENSE	46 71
TPC662	TP_PMU_AMUX_B7	71
TPC663	TP_PMU_AMUX_BY	71

TP of H9ML (EE tests)

TPC678	PCC_EVENT	38
TPC686	TP_SMC_DEBUG	46
TPC687	WLAN_CONTEXT_A	35 36 38
TPC688	WLAN_CONTEXT_B	35 36 38

TP of CONTEXT_A/B can be used for AOP_UART_TX/RX for debug

TPC600	LIDOPEN_PSU12VPGOOD_ACDCBURST_L	38 100
TPC6G8	SWD_SOC_SWDIO	38 46 113
TPC6G9	SWD_SOC_SWCLK	38 46 113

EE TESTS PCH

TPC631	PCIE_CLK100M_WLAN_PCH_N	12 20
TPC632	PCIE_CLK100M_WLAN_PCH_P	12 20
TPC633	PCIE_CLK100M_SOC_N	12 40
TPC634	PCIE_CLK100M_SOC_P	12 40
TPC637	PCIE_CLK100M_TBT_X_N	12 26
TPC638	PCIE_CLK100M_TBT_X_P	12 26
TPC639	PCIE_CLK100M_TBT_T_N	12 92
TPC640	PCIE_CLK100M_TBT_T_P	12 92
TPC690	SPI_PCHROM_MOSI	13 18
TPC691	TP_PCH_CLK32K_SUS	12
TPC692	SPI_IO<2>	13 18
TPC693	SPI_IO<3>	13

TP Debug ACE Nets (EE tests)

TPC622	UPC_XA_DEBUGUART_TX	29
TPC623	PMU_ACTIVE_READY	29 37 71 106 110
TPC624	UPC_XB_DEBUGUART_TX	30
TPC625	UPC_XB_GPIO1	30

Test Points for Ace XA/XB GPIO0/1, must have in production.

TPC626	UPC_TA_DEBUGUART_TX	95
TPC627	UPC_TA_GPIO1	95
TPC628	UPC_TB_DEBUGUART_TX	96
TPC629	UPC_TB_GPIO1	96

Test Points for Ace XA/XB GPIO0/1, must have in production.

SENSOR TPs

TPC694	SNS_P12VG3H_P	51
TPC695	SNS_P12VG3H_N	51
TPC6C9	ISNS_HS_COMPUTING_P	51
TPC6C8	ISNS_HS_COMPUTING_N	51
TPC6D2	CPUVR_ISNS_R_P	52
TPC6D1	CPUVR_ISNS_R_N	52
TPC6D0	ISNS_P3V3_G3W_SSD0_P	53
TPC6D3	ISNS_P3V3_G3W_SSD0_N	53
TPC6D6	ISNS_PPBUS_MAIN_SSD0_P	53
TPC6D5	ISNS_PPBUS_MAIN_SSD0_N	53
TPC6D4	ISNS_TBT_P	54
TPC6D8	ISNS_TBT_N	54
TPC6D7	ISNS_CPUVCCIO_P	54
TPC6E0	ISNS_CPUVCCIO_N	54
TPC6E1	CPUGT_ISNS_P	54
TPC6D9	CPUGT_ISNS_N	54
TPC6E4	ISNS_P5V_USBC_P	56
TPC6E3	ISNS_P5V_USBC_N	56
TPC6E2	ISNS_P5V_USBA_P	56
TPC6E6	ISNS_P5V_USBA_N	56
TPC6E5	ISNS_P3V3_ENET_P	56
TPC6E8	ISNS_P3V3_ENET_N	56
TPC6E9	ISNS_P12V_ENET_P	56
TPC6E7	ISNS_P12V_ENET_N	56
TPC6F0	PMU_CPUSA_VSENSE	46 56
TPC6F1	SMC_CPU_VCC_VSENSE	46 56
TPC6F4	SMC_CPUGT_VSENSE	46 56
TPC6F2	TSNS_T1_DX1_P	55
TPC6F3	TSNS_T1_DX2_P	55
TPC6F6	TSNS_T1_DX3_P	55
TPC6F7	TSNS_T1_DX4_P	55
TPC6F5	TSNS_T1_DX5_P	55
TPC6F9	TSNS_T1_DX6_P	55
TPC6F8	TSNS_T1_DX7_P	55
TPC6G0	TSNS_T1_DX8_P	55
TPC6G1	TSNS_T1_DN	55
TPC6G2	TSNS_T2_DX1_P	55
TPC6G4	TSNS_T2_DX4_P	55
TPC6G3	TSNS_T2_DX4_N	55
TPC6G5	TSNS_T2_DN	55
TPC6G6	TBTTHMSNS_X_D2_P	55
TPC6G7	TBTTHMSNS_X_D2_N	55
TPC6H1	REG_VCCSA_ISNS_1_P	54 66
TPC6H0	REG_VCCSA_ISNS_1_N	54 66
TPC6H3	ISNS_2V5_S3_P	52
TPC6H2	ISNS_2V5_S3_N	52
TPC6H5	TBTTHMSNS_T_D3_P	55
TPC6H4	TBTTHMSNS_T_D3_N	55

S4E

TPC619	SSD0_CLKREQ0_L	40 46 75
TPC617	SSD0_CLKREQ1_L	40 46 76
TPC616	SSD0_CLKREQ2_L	40 46 77
TPC630	SSD0_CLKREQ3_L	40 46 78
TPC614	SSD0_S4E0_DROOP_L	75
TPC618	SSD0_S4E1_DROOP_L	76
TPC611	SSD0_S4E2_DROOP_L	77
TPC612	SSD0_S4E3_DROOP_L	78
TPC685	SSD0_OCARINA_VDD_LDO	79
TPC689	SSD0_OCARINA_WP_L	75 76 77 78 79
TPC601	SSD0_VR_P2V7_EN	79
TPC602	SSD0_OCARINA_RESET_L	75 76 77 78 79
TPC603	SSD0_VR_P2V7_PGOOD	79
TPC604	SSD0_OCARINA_TCAL	79
TPC606	SSD0_OCARINA_PFN	75 76 77 78 79
TPC605	SSD0_OCARINA_FORCE_EN	79
TPC607	SSD0_OCARINA_VREF	79
TPC608	SSD0_S4E_BOOT2	74 75 76 77 78
TPC609	SSD0_S4E0_ZQ_C	75
TPC615	SSD0_S4E0_ZQ_L	75
TPC610	SSD0_S4E1_ZQ_C	76
TPC613	SSD0_S4E1_ZQ_L	76
TPC620	SSD0_S4E2_ZQ_C	77
TPC666	SSD0_S4E2_ZQ_L	77
TPC621	SSD0_S4E3_ZQ_C	78
TPC696	SSD0_S4E3_ZQ_L	78
TPC697	SSD0_S4E0_PCIE_RESREF	75
TPC698	SSD0_S4E1_PCIE_RESREF	76
TPC6A1	SSD0_S4E2_PCIE_RESREF	77
TPC6A0	SSD0_S4E3_PCIE_RESREF	78
TPC699	I2C_SSD_SCL	38 48
TPC6A2	I2C_SSD_SDA	38 48
TPC6A3	SSD_BFH	37 74 75 76 77 78
TPC6A4	SSD0_PCIE_RESET_L	40 46 75 76 77 78
TPC6A5	SSD0_STG01_ADDR	79
TPC6B0	TP_SSD0_OCARINA_VR2_DIS	79
TPC6B1	SSD0_OCARINA_LPB_L	74 75 76 77 78 79

SSD BOUNDARY SCAN Test-Points

TPC6A6	SSD0_S4E_JTAG_TRST_L	74 75 76 77 78
TPC6A9	SSD0_S4E_JTAG_SEL	74 75 76 77 78
TPC6A8	SSD0_SWDIO_UART_D2R	38 74 75 76 77 78
TPC6A7	SSD0_SWCLK_UART_R2D	38 74 75 76 77 78
TPC6B2	TP_SSD0_S4E0_ANI1_VREF	75
TPC6B3	TP_SSD0_S4E0_ANI0_VREF	75
TPC6B6	TP_SSD0_S4E1_ANI1_VREF	76
TPC6B5	TP_SSD0_S4E1_ANI0_VREF	76
TPC6B4	TP_SSD0_S4E2_ANI1_VREF	77
TPC6B7	TP_SSD0_S4E2_ANI0_VREF	77
TPC6B8	TP_SSD0_S4E3_ANI1_VREF	78
TPC6B9	TP_SSD0_S4E3_ANI0_VREF	78
TPC6C1	SSD0_S4E0_SWD_UID0	75
TPC6C0	SSD0_S4E0_SWD_UID1	75
TPC6C2	SSD0_S4E1_SWD_UID0	76
TPC6C3	SSD0_S4E1_SWD_UID1	76
TPC6C4	SSD0_S4E2_SWD_UID0	77
TPC6C6	SSD0_S4E2_SWD_UID1	77
TPC6C7	SSD0_S4E3_SWD_UID0	78
TPC6C5	SSD0_S4E3_SWD_UID1	78

BOM_COST_GROUP=PCB

PAGE TITLE: ICT, MAC-1 ,EE Testpoints

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ICT TESTPOINTS , High Speed NO_TEST

CPU

PEG

84 5	IN	PCIE ENET D2R N<3..0>	NO_TEST=1
84 5	IN	PCIE ENET D2R P<3..0>	NO_TEST=1
84 5	IN	PCIE ENET R2D C N<3..0>	NO_TEST=1
84 5	IN	PCIE ENET R2D C P<3..0>	NO_TEST=1
94 5	IN	PCIE TBT T D2R N<3..0>	NO_TEST=1
94 5	IN	PCIE TBT T D2R P<3..0>	NO_TEST=1
94 5	IN	PCIE TBT T R2D C N<3..0>	NO_TEST=1
94 5	IN	PCIE TBT T R2D C P<3..0>	NO_TEST=1
28 5	IN	PCIE TBT X D2R N<3..0>	NO_TEST=1
28 5	IN	PCIE TBT X D2R P<3..0>	NO_TEST=1
28 5	IN	PCIE TBT X R2D C N<3..0>	NO_TEST=1
28 5	IN	PCIE TBT X R2D C P<3..0>	NO_TEST=1

DMI

13 5	IN	DMI S2N N<3..0>	NO_TEST=1
13 5	IN	DMI S2N P<3..0>	NO_TEST=1
13 5	IN	DMI N2S N<3..0>	NO_TEST=1
13 5	IN	DMI N2S P<3..0>	NO_TEST=1

DDI

21 5	IN	DP DDI1 ML C N<3..0>	NO_TEST=1
21 5	IN	DP DDI1 ML C P<3..0>	NO_TEST=1
21 5	IN	DP DDI2 ML C N<3..0>	NO_TEST=1
21 5	IN	DP DDI2 ML C P<3..0>	NO_TEST=1
91 5	IN	DP DDI3 ML C N<3..0>	NO_TEST=1
91 5	IN	DP DDI3 ML C P<3..0>	NO_TEST=1
21 5	IN	DP DDI1 AUXCH C N	NO_TEST=1
21 5	IN	DP DDI1 AUXCH C P	NO_TEST=1
21 5	IN	DP DDI2 AUXCH C N	NO_TEST=1
21 5	IN	DP DDI2 AUXCH C P	NO_TEST=1
91 5	IN	DP DDI3 AUXCH C N	NO_TEST=1
91 5	IN	DP DDI3 AUXCH C P	NO_TEST=1

CPU CLK

12 6	IN	CPU CLK24M NSSC CLK N	NO_TEST=1
12 6	IN	CPU CLK24M NSSC CLK P	NO_TEST=1
12 6	IN	CPU CLK100M PCIBCLK N	NO_TEST=1
12 6	IN	CPU CLK100M PCIBCLK P	NO_TEST=1
12 6	IN	CPU CLK100M BCLK N	NO_TEST=1
12 6	IN	CPU CLK100M BCLK P	NO_TEST=1

DDR4 MEM

25 7	IN	MEM A DQ<63..0>	NO_TEST=1
25 7	IN	MEM A DQS N<7..0>	NO_TEST=1
25 7	IN	MEM A DQS P<7..0>	NO_TEST=1
23 7	IN	MEM A CLK N<1..0>	NO_TEST=1
23 7	IN	MEM A CLK P<1..0>	NO_TEST=1
23 7	IN	MEM A CKE<1..0>	NO_TEST=1
23 7	IN	MEM A CS L<1..0>	NO_TEST=1
23 7	IN	MEM A ODT<1..0>	NO_TEST=1
23 7	IN	MEM A BA<1..0>	NO_TEST=1
23 7	IN	MEM A BG<1..0>	NO_TEST=1
23 7	IN	MEM A ACT L	NO_TEST=1
23 7	IN	MEM A ALERT L	NO_TEST=1
23 7	IN	MEM A PAR	NO_TEST=1
23 7	IN	MEM A A<16..0>	NO_TEST=1
25 7	IN	MEM B DQ<63..0>	NO_TEST=1
25 7	IN	MEM B DQS N<7..0>	NO_TEST=1
25 7	IN	MEM B DQS P<7..0>	NO_TEST=1
24 7	IN	MEM B CLK N<1..0>	NO_TEST=1
24 7	IN	MEM B CLK P<1..0>	NO_TEST=1
24 7	IN	MEM B CKE<1..0>	NO_TEST=1
24 7	IN	MEM B CS L<1..0>	NO_TEST=1
24 7	IN	MEM B ODT<1..0>	NO_TEST=1
24 7	IN	MEM B BA<1..0>	NO_TEST=1
24 7	IN	MEM B BG<1..0>	NO_TEST=1
24 7	IN	MEM B ACT L	NO_TEST=1
24 7	IN	MEM B ALERT L	NO_TEST=1
24 7	IN	MEM B PAR	NO_TEST=1
24 7	IN	MEM B A<16..0>	NO_TEST=1

PMIC

XTAL

71	IN	PMU XTAL1	NO_TEST=1
71	IN	PMU XTAL1 R	NO_TEST=1
71	IN	PMU XTAL2	NO_TEST=1

PCH

CLK

18 12	IN	ITPXDP CLK100M N	NO_TEST=1
18 12	IN	ITPXDP CLK100M P	NO_TEST=1

USB 3.0

113 109 14	IN	USB3 VITAMIN D2R N	NO_TEST=1
113 109 14	IN	USB3 VITAMIN D2R P	NO_TEST=1
113 109 14	IN	USB3 VITAMIN D2R N	NO_TEST=1
113 109 14	IN	USB3 VITAMIN D2R P	NO_TEST=1
113 14	IN	USB3 VITAMIN R2D C N	NO_TEST=1
113 14	IN	USB3 VITAMIN R2D C P	NO_TEST=1
62 14	IN	USB3 EXTA D2R N	NO_TEST=1
62 14	IN	USB3 EXTA D2R P	NO_TEST=1
62 14	IN	USB3 EXTA R2D C N	NO_TEST=1
62 14	IN	USB3 EXTA R2D C P	NO_TEST=1
62 14	IN	USB3 EXTB D2R N	NO_TEST=1
62 14	IN	USB3 EXTB D2R P	NO_TEST=1
62 14	IN	USB3 EXTB R2D C N	NO_TEST=1
62 14	IN	USB3 EXTB R2D C P	NO_TEST=1

PCIE

20 14	IN	PCIE WLANPCH D2R N	NO_TEST=1
20 14	IN	PCIE WLANPCH D2R P	NO_TEST=1
20 14	IN	PCIE WLANPCH R2D C N	NO_TEST=1
20 14	IN	PCIE WLANPCH R2D C P	NO_TEST=1
81 14	IN	PCIE ENET PCH D2R N	NO_TEST=1
81 14	IN	PCIE ENET PCH D2R P	NO_TEST=1
81 14	IN	PCIE ENET PCH R2D C N	NO_TEST=1
81 14	IN	PCIE ENET PCH R2D C P	NO_TEST=1
40 14	IN	PCIE SOC D2R N<3..0>	NO_TEST=1
40 14	IN	PCIE SOC D2R P<3..0>	NO_TEST=1
46 14	IN	PCIE SOC R2D C N<3..0>	NO_TEST=1
46 14	IN	PCIE SOC R2D C P<3..0>	NO_TEST=1

PCIE

19	IN	PCH CLK24M XTALOUT R	NO_TEST=1
19 12	IN	PCH CLK24M XTALIN	NO_TEST=1
19 12	IN	PCH CLK24M XTALOUT	NO_TEST=1

Display MUX

DP

92 21	IN	DP T SNK1 ML C N<3..0>	NO_TEST=1
92 21	IN	DP T SNK1 ML C P<3..0>	NO_TEST=1
92 21	IN	DP T SNK0 ML C N<3..0>	NO_TEST=1
92 21	IN	DP T SNK0 ML C P<3..0>	NO_TEST=1
92 21	IN	DP T SNK1 AUXCH C N	NO_TEST=1
92 21	IN	DP T SNK1 AUXCH C P	NO_TEST=1
92 21	IN	DP T SNK0 AUXCH C N	NO_TEST=1
92 21	IN	DP T SNK0 AUXCH C P	NO_TEST=1
26 21	IN	DP X SNK1 ML C N<3..0>	NO_TEST=1
26 21	IN	DP X SNK1 ML C P<3..0>	NO_TEST=1
26 21	IN	DP X SNK0 ML C N<3..0>	NO_TEST=1
26 21	IN	DP X SNK0 ML C P<3..0>	NO_TEST=1
26 21	IN	DP X SNK1 AUXCH C N	NO_TEST=1
26 21	IN	DP X SNK1 AUXCH C P	NO_TEST=1
26 21	IN	DP X SNK0 AUXCH C N	NO_TEST=1
26 21	IN	DP X SNK0 AUXCH C P	NO_TEST=1

SSD

PCIE

78 77 76 75	IN	PCIE SSD0 D2R C N<3..0>	NO_TEST=1
78 77 76 75	IN	PCIE SSD0 D2R C P<3..0>	NO_TEST=1
78 77 76 75	IN	PCIE SSD0 R2D N<3..0>	NO_TEST=1
78 77 76 75	IN	PCIE SSD0 R2D P<3..0>	NO_TEST=1

Titan Ridges

PCIE

28 26	IN	PCIE TBT X R2D N<3..0>	NO_TEST=1
28 26	IN	PCIE TBT X R2D P<3..0>	NO_TEST=1
28 26	IN	PCIE TBT X D2R C N<3..0>	NO_TEST=1
28 26	IN	PCIE TBT X D2R C P<3..0>	NO_TEST=1
94 92	IN	PCIE TBT T R2D N<3..0>	NO_TEST=1
94 92	IN	PCIE TBT T R2D P<3..0>	NO_TEST=1
94 92	IN	PCIE TBT T D2R C N<3..0>	NO_TEST=1
94 92	IN	PCIE TBT T D2R C P<3..0>	NO_TEST=1

DP

26	IN	DP X SNK0 ML N<3..0>	NO_TEST=1
26	IN	DP X SNK0 ML P<3..0>	NO_TEST=1
26	IN	DP X SNK0 AUXCH N	NO_TEST=1
26	IN	DP X SNK0 AUXCH P	NO_TEST=1
26	IN	DP X SNK1 ML N<3..0>	NO_TEST=1
26	IN	DP X SNK1 ML P<3..0>	NO_TEST=1
26	IN	DP X SNK1 AUXCH N	NO_TEST=1
26	IN	DP X SNK1 AUXCH P	NO_TEST=1
92	IN	DP T SNK0 ML N<3..0>	NO_TEST=1
92	IN	DP T SNK0 ML P<3..0>	NO_TEST=1
92	IN	DP T SNK0 AUXCH N	NO_TEST=1
92	IN	DP T SNK0 AUXCH P	NO_TEST=1
92	IN	DP T SNK1 ML N<3..0>	NO_TEST=1
92	IN	DP T SNK1 ML P<3..0>	NO_TEST=1
92	IN	DP T SNK1 AUXCH N	NO_TEST=1
92	IN	DP T SNK1 AUXCH P	NO_TEST=1

USB-C

31 26	IN	USBC XA D2R N<2..1>	NO_TEST=1
31 26	IN	USBC XA D2R P<2..1>	NO_TEST=1
31 26	IN	USBC XA R2D C N<2..1>	NO_TEST=1
31 26	IN	USBC XA R2D C P<2..1>	NO_TEST=1
31 26	IN	USBC XB D2R N<2..1>	NO_TEST=1
31 26	IN	USBC XB D2R P<2..1>	NO_TEST=1
31 26	IN	USBC XB R2D C N<2..1>	NO_TEST=1
31 26	IN	USBC XB R2D C P<2..1>	NO_TEST=1
97 92	IN	USBC TA D2R N<2..1>	NO_TEST=1
97 92	IN	USBC TA D2R P<2..1>	NO_TEST=1
97 92	IN	USBC TA R2D C N<2..1>	NO_TEST=1
97 92	IN	USBC TA R2D C P<2..1>	NO_TEST=1
97 92	IN	USBC TB D2R N<2..1>	NO_TEST=1
97 92	IN	USBC TB D2R P<2..1>	NO_TEST=1
97 92	IN	USBC TB R2D C N<2..1>	NO_TEST=1
97 92	IN	USBC TB R2D C P<2..1>	NO_TEST=1

XTAL

28 26	IN	TBT X XTAL25M OUT	NO_TEST=1
28 26	IN	TBT X XTAL25M IN	NO_TEST=1
28	IN	TBT X XTAL25M OUT R	NO_TEST=1

Madea

DP

91 90	IN	LPDPTX DATA N<3..0>	NO_TEST=1
91 90	IN	LPDPTX DATA P<3..0>	NO_TEST=1
91 90	IN	LPDPTX AUX N	NO_TEST=1
91 90	IN	LPDPTX AUX P	NO_TEST=1

HDMI

90 89	IN	HDMI DATA N<2..0>	NO_TEST=1
90 89	IN	HDMI DATA P<2..0>	NO_TEST=1
89 88	IN	HDMI DATA CONN N<2..0>	NO_TEST=1
89 88	IN	HDMI DATA CONN P<2..0>	NO_TEST=1
89 88	IN	HDMI CLK CONN N	NO_TEST=1
89 88	IN	HDMI CLK CONN P	NO_TEST=1
89	IN	HDMI CLK FLT N	NO_TEST=1
89	IN	HDMI CLK FLT P	NO_TEST=1
89	IN	HDMI CLK R N	NO_TEST=1
89	IN	HDMI CLK R P	NO_TEST=1
90 89	IN	HDMI CLK N	NO_TEST=1
90 89	IN	HDMI CLK P	NO_TEST=1

USB-C CONN

USB-C

31	IN	USBC XA D2R RC N<2..1>	NO_TEST=1
31	IN	USBC XA D2R RC P<2..1>	NO_TEST=1
31	IN	USBC XA R2D RC N<2..1>	NO_TEST=1
31	IN	USBC XA R2D RC P<2..1>	NO_TEST=1
31	IN	USBC XA D2R CONN N<2..1>	NO_TEST=1
31	IN	USBC XA D2R CONN P<2..1>	NO_TEST=1
31	IN	USBC XA R2D CONN N<2..1>	NO_TEST=1
31	IN	USBC XA R2D CONN P<2..1>	NO_TEST=1
31 28	IN	USBC XA USB DBG TOP N	NO_TEST=1
31 28	IN	USBC XA USB DBG TOP P	NO_TEST=1
31 28	IN	USBC XA USB DBG BOT N	NO_TEST=1
31 28	IN	USBC XA USB DBG BOT P	NO_TEST=1
31	IN	USBC XB D2R RC N<2..1>	NO_TEST=1
31	IN	USBC XB D2R RC P<2..1>	NO_TEST=1
31	IN	USBC XB R2D RC N<2..1>	NO_TEST=1
31	IN	USBC XB R2D RC P<2..1>	NO_TEST=1
31	IN	USBC XB D2R CONN N<2..1>	NO_TEST=1
31	IN	USBC XB D2R CONN P<2..1>	NO_TEST=1
31	IN	USBC XB R2D CONN N<2..1>	NO_TEST=1
31	IN	USBC XB R2D CONN P<2..1>	NO_TEST=1
31 30	IN	USBC XB USB TOP N	NO_TEST=1
31 30	IN	USBC XB USB TOP P	NO_TEST=1
31 30	IN	USBC XB USB BOT N	NO_TEST=1
31 30	IN	USBC XB USB BOT P	NO_TEST=1
97	IN	USBC TA D2R RC N<2..1>	NO_TEST=1
97	IN	USBC TA D2R RC P<2..1>	NO_TEST=1
97	IN	USBC TA R2D RC N<2..1>	NO_TEST=1
97	IN	USBC TA R2D RC P<2..1>	NO_TEST=1
97	IN	USBC TA D2R CONN N<2..1>	NO_TEST=1
97	IN	USBC TA D2R CONN P<2..1>	NO_TEST=1
97	IN	USBC TA R2D CONN N<2..1>	NO_TEST=1
97	IN	USBC TA R2D CONN P<2..1>	NO_TEST=1
97 95	IN	USBC TA USB TOP N	NO_TEST=1
97 95	IN	USBC TA USB TOP P	NO_TEST=1
97 95	IN	USBC TA USB BOT N	NO_TEST=1
97 95	IN	USBC TA USB BOT P	NO_TEST=1
97	IN	USBC TB D2R RC N<2..1>	NO_TEST=1
97	IN	USBC TB D2R RC P<2..1>	NO_TEST=1
97	IN	USBC TB R2D RC N<2..1>	NO_TEST=1
97	IN	USBC TB R2D RC P<2..1>	NO_TEST=1
97	IN	USBC TB D2R CONN N<2..1>	NO_TEST=1
97	IN	USBC TB D2R CONN P<2..1>	NO_TEST=1
97	IN	USBC TB R2D CONN N<2..1>	NO_TEST=1
97	IN	USBC TB R2D CONN P<2..1>	NO_TEST=1
97 96	IN	USBC TB USB TOP N	NO_TEST=1
97 96	IN	USBC TB USB TOP P	NO_TEST=1
97 96	IN	USBC TB USB BOT N	NO_TEST=1
97 96	IN	USBC TB USB BOT P	NO_TEST=1

Harpoon

ANT MATCH

36 35	IN	50 G 0 MATCH	NO_TEST=1
36 35	IN	50 A 0 MATCH	NO_TEST=1
36 35	IN	50 G 1 MATCH	NO_TEST=1
36 35	IN	50 A 1 MATCH	NO_TEST=1
36 35	IN	50 G 2 MATCH	NO_TEST=1
36 35	IN	50 A 2 MATCH	NO_TEST=1
36	IN	50 G 0 DIPLEXER	NO_TEST=1
36	IN	50 A 0 DIPLEXER	NO_TEST=1
36	IN	50 G 1 DIPLEXER	NO_TEST=1
36	IN	50 A 1 DIPLEXER	NO_TEST=1
36	IN	50 G 2 DIPLEXER	NO_TEST=1
36	IN	50 A 2 DIPLEXER	NO_TEST=1
36	IN	50 0 COM	NO_TEST=1
36	IN	50 0 ANT	NO_TEST=1
36	IN	50 1 COM	NO_TEST=1
36	IN	50 1 ANT	NO_TEST=1
36	IN	50 2 COM	NO_TEST=1
36	IN	50 2 ANT	NO_TEST=1

PCIE

35	IN	PCH PCIE WLAN D2R C N	NO_TEST=1
35	IN	PCH PCIE WLAN D2R C P	NO_TEST=1
35	IN	PCH PCIE WLAN R2D N	NO_TEST=1
35	IN	PCH PCIE WLAN R2D P	NO_TEST=1

BOM_COST_GROUP=PCB

H9M

PCIE

46 40	IN	PCIE SOC R2D N<3..0>	NO_TEST=1
46 40	IN	PCIE SOC R2D P<3..0>	NO_TEST=1
40	IN	PCIE SOC D2R C N<3..0>	NO_TEST=1
40	IN	PCIE SOC D2R C P<3..0>	NO_TEST=1

SSD PCIE

78 77 76 75 40	IN	PCIE SSD0 D2R N<3..0>	NO_TEST=1
78 77 76 75 40	IN	PCIE SSD0 D2R P<3..0>	NO_TEST=1
78 77 76 75 40	IN	PCIE SSD0 R2D C N<3..0>	NO_TEST=1
78 77 76 75 40	IN	PCIE SSD0 R2D C P<3..0>	NO_TEST=1

ESPI

38	IN	ESPI IO R<3..0>	NO_TEST=1
113 38 12	IN	ESPI IO<3..0>	NO_TEST=1
113 38 12	IN	ESPI CLK	NO_TEST=1
12	IN	ESPI CLK60M R	NO_TEST=1

XTAL

37	IN	SOC XTAL24M OUT	NO_TEST=1
37	IN	SOC XTAL24M IN	NO_TEST=1
37	IN	SOC XTAL24M OUT R	NO_TEST=1

ENET

PCIE

81 80	IN	PCIE ENET 1G D2R C N	NO_TEST=1
81 80	IN	PCIE ENET 1G D2R C P	NO_TEST=1
81 80	IN	PCIE ENET 1G R2D N	NO_TEST=1
81 80	IN	PCIE ENET 1G R2D P	NO_TEST=1
84 82	IN	PCIE ENET D2R C P<3..0>	NO_TEST=1
84 82	IN	PCIE ENET D2R C N<3..0>	NO_TEST=1
84 82	IN	PCIE ENET R2D N<3..0>	NO_TEST=1
84 82	IN	PCIE ENET R2D P<3..0>	NO_TEST=1

MDI

85 80	IN	ENETCONN MDI N<3..0>	NO_TEST=1
85 80	IN	ENETCONN MDI P<3..0>	NO_TEST=1
85	IN	ENET A N R	NO_TEST=1
85	IN	ENET A P R	NO_TEST=1
85	IN	ENET A CMC N	NO_TEST=1
85	IN	ENET A CMC P	NO_TEST=1
107 85	IN	ENET CONN A N	NO_TEST=1
107 85	IN	ENET CONN A P	NO_TEST=1
85	IN	ENET B N R	NO_TEST=1
85	IN	ENET B P R	NO_TEST=1
85	IN	ENET B CMC N	NO_TEST=1
85	IN	ENET B CMC P	NO_TEST=1
107 85	IN	ENET CONN B N	NO_TEST=1
107 85	IN	ENET CONN B P	NO_TEST=1
85	IN	ENET C N R	NO_TEST=1
85	IN	ENET C P R	NO_TEST=1
85	IN	ENET C CMC N	NO_TEST=1
85	IN	ENET C CMC P	NO_TEST=1
107 85	IN	ENET CONN C N	NO_TEST=1
107 85	IN	ENET CONN C P	NO_TEST=1
85	IN	ENET D N R	NO_TEST=1
85	IN	ENET D P R	NO_TEST=1
85	IN	ENET D CMC N	NO_TEST=1
85	IN	ENET D CMC P	NO_TEST=1
107 85	IN	ENET CONN D N	NO_TEST=1
107 85	IN	ENET CONN D P	NO_TEST=1
85 82	IN	ENET A N	NO_TEST=1
85 82	IN	ENET A P	NO_TEST=1
85 82	IN	ENET B N	NO_TEST=1
85 82	IN	ENET B P	NO_TEST=1
85 82	IN	ENET C N	NO_TEST=1
85 82	IN	ENET C P	NO_TEST=1
85 82	IN	ENET D N	NO_TEST=1
85 82	IN	ENET D P	NO_TEST=1

PAGE TITLE
High speed No Testpoints

Apple Inc.

DRAWING NUMBER 051-02424
SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 127 OF 142
SHEET 109 OF 115

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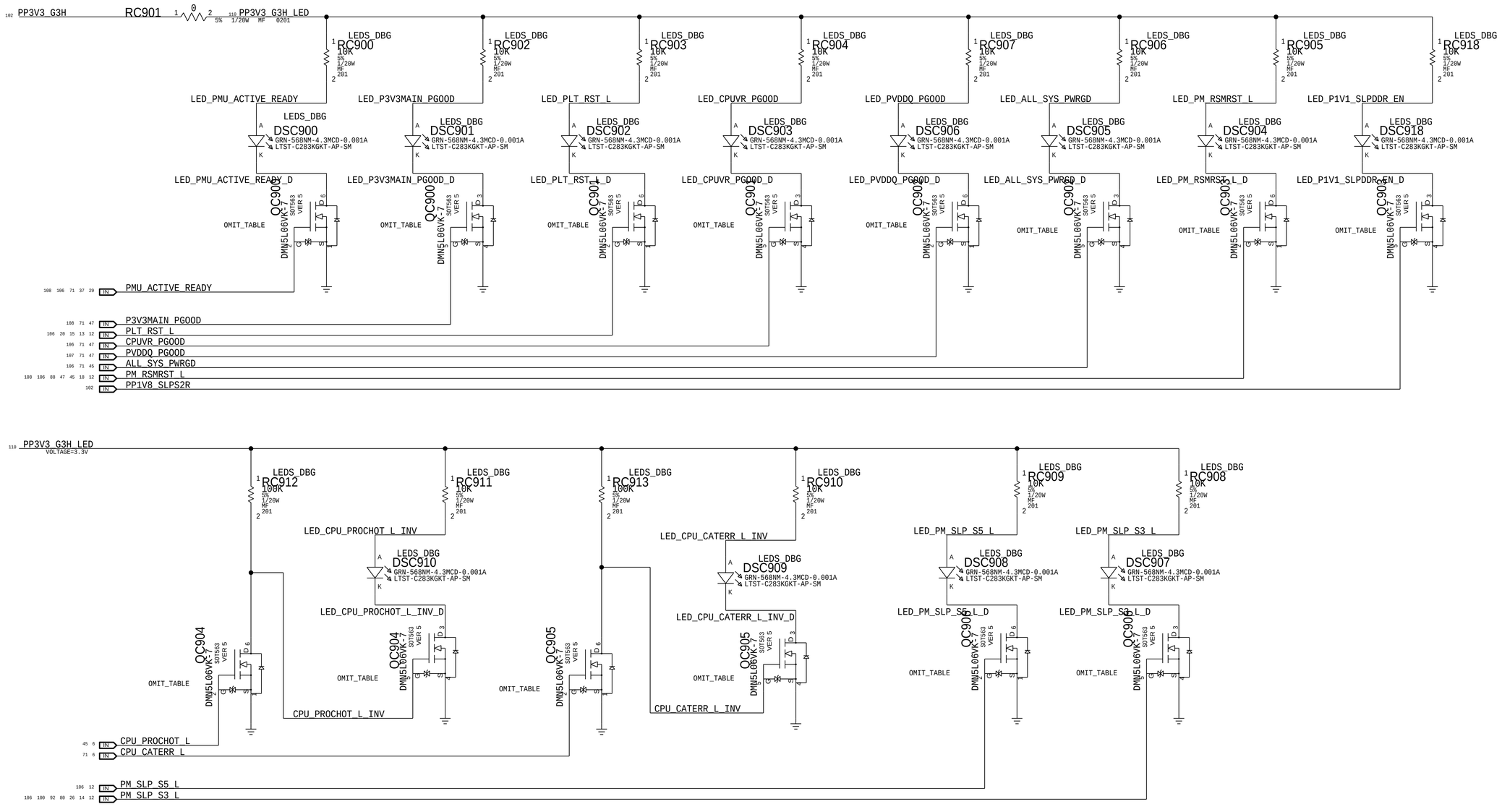

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00074	7	dual FET	QC900,QC901,QC902,QC903,QC904,QC905,QC906	CRITICAL	LEDS_DBG

BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE

DEBUG LEDS

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BOM_COST_GROUP=PCB

PAGE TITLE

Constraints

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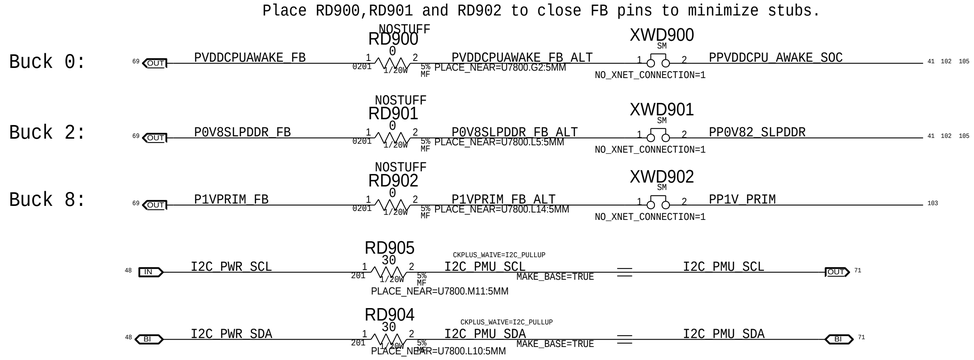
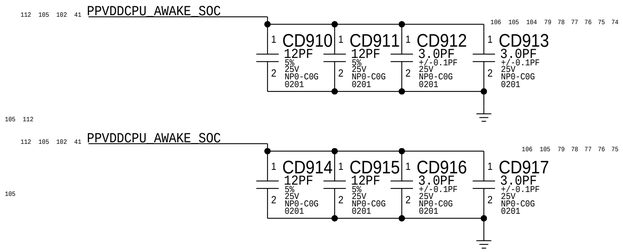
Calpe Dev Support:

Alternate Feedback:remote sense

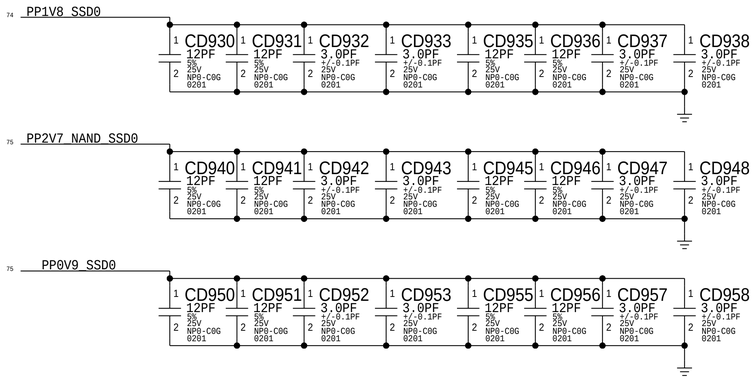
Place RD900,RD901 and RD902 to close FB pins to minimize stubs.



H9ML Desense Caps:



SSD/NAND Desense Caps:



BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

PAGE TITLE: Dev Support 1

Apple Inc.

DRAWING NUMBER: 051-02424 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 139 OF 142

SHEET: 112 OF 115

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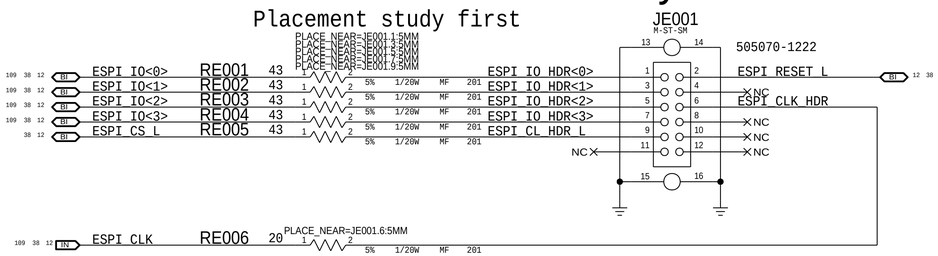
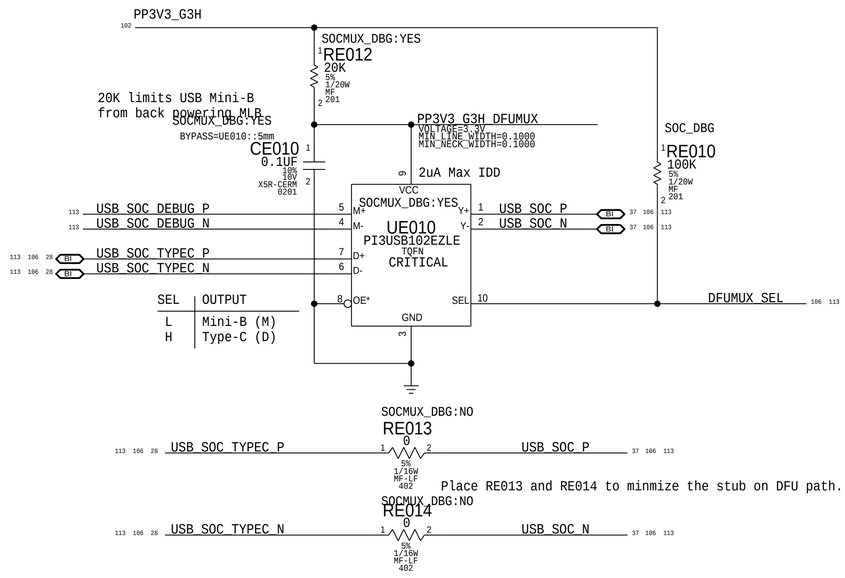
eSPI Analyzer

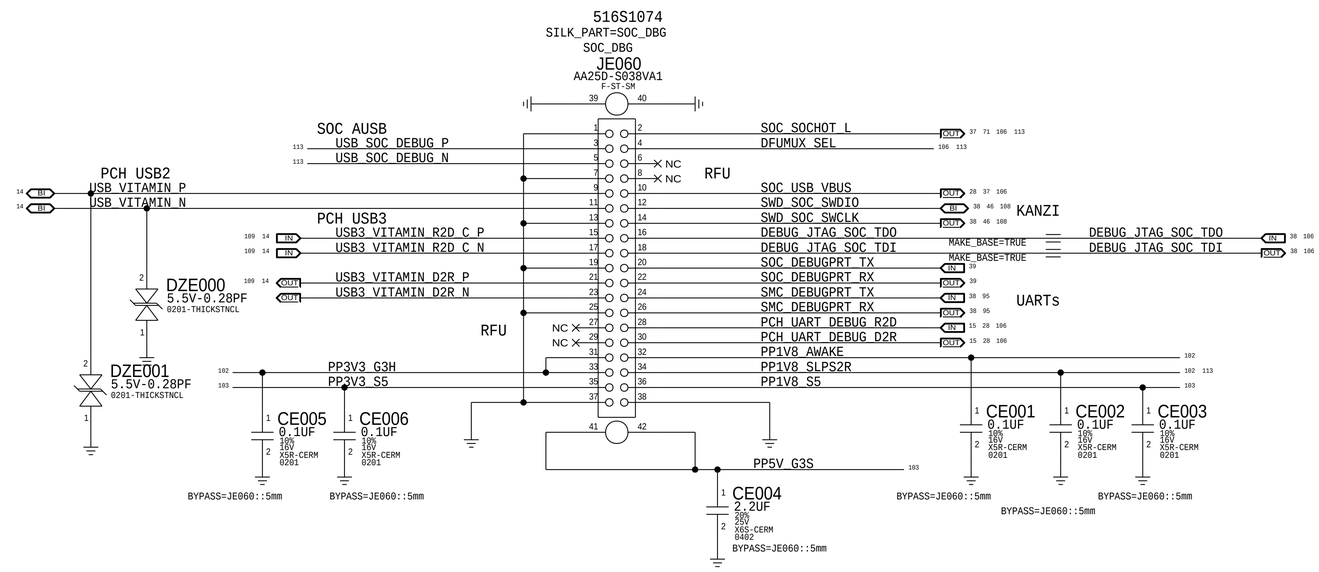
Placement study first



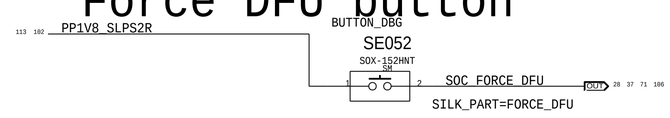
SoC USB DFU Mux



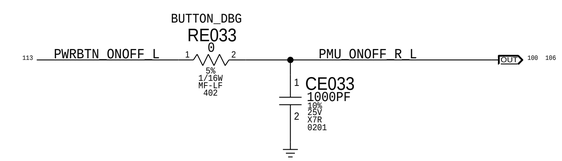
SOC DEBUG Connector



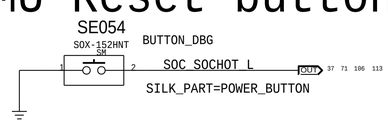
Force DFU button



Debug Power button



PMU Reset button



BOM_COST_GROUP=DEBUG

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

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Apple Inc.

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BOM Variants

	BOM NUMBER	BOM NAME	BOM OPTIONS
-->	639-06831	PCBA,MLB,3.6G_4C,X1036,128G_WD,ENET_1G	COMM_BOM,CPU:3.6G,SSD:128_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06830	PCBA,MLB,3.6G_4C,X1036,128G_TB,ENET_1G	COMM_BOM,CPU:3.6G,SSD:128_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06849	PCBA,MLB,3.6G_4C,X1036,256G_WD,ENET_1G	COMM_BOM,CPU:3.6G,SSD:256_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06832	PCBA,MLB,3.6G_4C,X1036,256G_TB,ENET_1G	COMM_BOM,CPU:3.6G,SSD:256_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06833	PCBA,MLB,3.6G_4C,X1036,512G_WD,ENET_1G	COMM_BOM,CPU:3.6G,SSD:512_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06834	PCBA,MLB,3.6G_4C,X1036,512G_TB,ENET_1G	COMM_BOM,CPU:3.6G,SSD:512_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06835	PCBA,MLB,3.6G_4C,X1036,1TB_WD,ENET_1G	COMM_BOM,CPU:3.6G,SSD:1T_SD,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06836	PCBA,MLB,3.6G_4C,X1036,1TB_TB,ENET_1G	COMM_BOM,CPU:3.6G,SSD:1T_TB,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06837	PCBA,MLB,3.6G_4C,X1036,2TB_SM,ENET_1G	COMM_BOM,CPU:3.6G,SSD:2T_SM,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
3.6GHz, ENET_10G->			
	639-06838	PCBA,MLB,3.6G_4C,X1036,128G_WD,ENET_10G	COMM_BOM,CPU:3.6G,SSD:128_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-06839	PCBA,MLB,3.6G_4C,X1036,128G_TB,ENET_10G	COMM_BOM,CPU:3.6G,SSD:128_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-06840	PCBA,MLB,3.6G_4C,X1036,256G_WD,ENET_10G	COMM_BOM,CPU:3.6G,SSD:256_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-06841	PCBA,MLB,3.6G_4C,X1036,256G_TB,ENET_10G	COMM_BOM,CPU:3.6G,SSD:256_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-06842	PCBA,MLB,3.6G_4C,X1036,512G_WD,ENET_10G	COMM_BOM,CPU:3.6G,SSD:512_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-06843	PCBA,MLB,3.6G_4C,X1036,512G_TB,ENET_10G	COMM_BOM,CPU:3.6G,SSD:512_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-06844	PCBA,MLB,3.6G_4C,X1036,1TB_WD,ENET_10G	COMM_BOM,CPU:3.6G,SSD:1T_SD,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-06845	PCBA,MLB,3.6G_4C,X1036,1TB_TB,ENET_10G	COMM_BOM,CPU:3.6G,SSD:1T_TB,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-06846	PCBA,MLB,3.6G_4C,X1036,2TB_SM,ENET_10G	COMM_BOM,CPU:3.6G,SSD:2T_SM,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
2.8GHz, ENET_1G->			
	639-05191	PCBA,MLB,2.8G,X1036,128G_WD,ENET_1G	COMM_BOM,CPU:2.8G,SSD:128_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05383	PCBA,MLB,2.8G,X1036,128G_TB,ENET_1G	COMM_BOM,CPU:2.8G,SSD:128_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05177	PCBA,MLB,2.8G,X1036,256G_WD,ENET_1G	COMM_BOM,CPU:2.8G,SSD:256_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05385	PCBA,MLB,2.8G,X1036,256G_TB,ENET_1G	COMM_BOM,CPU:2.8G,SSD:256_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05387	PCBA,MLB,2.8G,X1036,512G_WD,ENET_1G	COMM_BOM,CPU:2.8G,SSD:512_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05391	PCBA,MLB,2.8G,X1036,512G_TB,ENET_1G	COMM_BOM,CPU:2.8G,SSD:512_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05393	PCBA,MLB,2.8G,X1036,1TB_WD,ENET_1G	COMM_BOM,CPU:2.8G,SSD:1T_SD,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05397	PCBA,2.8G,MLB,X1036,1TB_TB,ENET_1G	COMM_BOM,CPU:2.8G,SSD:1T_TB,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05959	PCBA,MLB,2.8GHz,X1036,2TB_SM,ENET_1G	COMM_BOM,CPU:2.8G,SSD:2T_SM,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
2.8GHz, ENET_10G->			
	639-05189	PCBA,MLB,2.8G,X1036,128G_WD,ENET_10G	COMM_BOM,CPU:2.8G,SSD:128_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05384	PCBA,MLB,2.8G,X1036,128G_TB,ENET_10G	COMM_BOM,CPU:2.8G,SSD:128_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05175	PCBA,MLB,2.8G,X1036,256G_WD,ENET_10G	COMM_BOM,CPU:2.8G,SSD:256_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05386	PCBA,MLB,2.8G,X1036,256G_TB,ENET_10G	COMM_BOM,CPU:2.8G,SSD:256_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05388	PCBA,MLB,2.8G,X1036,512G_WD,ENET_10G	COMM_BOM,CPU:2.8G,SSD:512_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05392	PCBA,MLB,2.8G,X1036,512G_TB,ENET_10G	COMM_BOM,CPU:2.8G,SSD:512_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05394	PCBA,MLB,2.8G,X1036,1TB_WD,ENET_10G	COMM_BOM,CPU:2.8G,SSD:1T_SD,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05398	PCBA,2.8G,MLB,X1036,1TB_TB,ENET_10G	COMM_BOM,CPU:2.8G,SSD:1T_TB,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05958	PCBA,MLB,2.8GHz,X1036,2TB_SM,ENET_10G	COMM_BOM,CPU:2.8G,SSD:2T_SM,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
3.0GHz, ENET_1G->			
	639-05971	PCBA,MLB,3.0GHz,X1036,256G_SD,ENET_1G	COMM_BOM,CPU:3.0G,SSD:256_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05969	PCBA,MLB,3.0GHz,X1036,256G_TB,ENET_1G	COMM_BOM,CPU:3.0G,SSD:256_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05977	PCBA,MLB,3.0GHz,X1036,512G_SD,ENET_1G	COMM_BOM,CPU:3.0G,SSD:512_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05975	PCBA,MLB,3.0GHz,X1036,512G_TB,ENET_1G	COMM_BOM,CPU:3.0G,SSD:512_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05983	PCBA,MLB,3.0GHz,X1036,1T_SD,ENET_1G	COMM_BOM,CPU:3.0G,SSD:1T_SD,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05981	PCBA,MLB,3.0GHz,X1036,1T_TB,ENET_1G	COMM_BOM,CPU:3.0G,SSD:1T_TB,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05985	PCBA,MLB,3.0GHz,X1036,2T_SM,ENET_1G	COMM_BOM,CPU:3.0G,SSD:2T_SM,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
3.0GHz, ENET_10G->			
	639-05968	PCBA,MLB,3.0GHz,X1036,256G_SD,ENET_10G	COMM_BOM,CPU:3.0G,SSD:256_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05966	PCBA,MLB,3.0GHz,X1036,256G_TB,ENET_10G	COMM_BOM,CPU:3.0G,SSD:256_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05974	PCBA,MLB,3.0GHz,X1036,512G_SD,ENET_10G	COMM_BOM,CPU:3.0G,SSD:512_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05972	PCBA,MLB,3.0GHz,X1036,512G_TB,ENET_10G	COMM_BOM,CPU:3.0G,SSD:512_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05980	PCBA,MLB,3.0GHz,X1036,1T_SD,ENET_10G	COMM_BOM,CPU:3.0G,SSD:1T_SD,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05978	PCBA,MLB,3.0GHz,X1036,1T_TB,ENET_10G	COMM_BOM,CPU:3.0G,SSD:1T_TB,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05984	PCBA,MLB,3.0GHz,X1036,2T_SM,ENET_10G	COMM_BOM,CPU:3.0G,SSD:2T_SM,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
3.2GHz, ENET_1G->			
	639-05997	PCBA,MLB,3.2GHz,X1036,256G_SD,ENET_1G	COMM_BOM,CPU:3.2G,SSD:256_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-05995	PCBA,MLB,3.2GHz,X1036,256G_TB,ENET_1G	COMM_BOM,CPU:3.2G,SSD:256_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06003	PCBA,MLB,3.2GHz,X1036,512G_SD,ENET_1G	COMM_BOM,CPU:3.2G,SSD:512_SD,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06001	PCBA,MLB,3.2GHz,X1036,512G_TB,ENET_1G	COMM_BOM,CPU:3.2G,SSD:512_TB,X1036_ENET_1G,SOC:1G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06009	PCBA,MLB,3.2GHz,X1036,1T_SD,ENET_1G	COMM_BOM,CPU:3.2G,SSD:1T_SD,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06007	PCBA,MLB,3.2GHz,X1036,1T_TB,ENET_1G	COMM_BOM,CPU:3.2G,SSD:1T_TB,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
	639-06011	PCBA,MLB,3.2GHz,X1036,2T_SM,ENET_1G	COMM_BOM,CPU:3.2G,SSD:2T_SM,X1036_ENET_1G,SOC:2G_DEV,ALTERNATE,DEV_BOM,1GDBG_BOM
3.2GHz, ENET_10G->			
	639-05994	PCBA,MLB,3.2GHz,X1036,256G_SD,ENET_10G	COMM_BOM,CPU:3.2G,SSD:256_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05992	PCBA,MLB,3.2GHz,X1036,256G_TB,ENET_10G	COMM_BOM,CPU:3.2G,SSD:256_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-06000	PCBA,MLB,3.2GHz,X1036,512G_SD,ENET_10G	COMM_BOM,CPU:3.2G,SSD:512_SD,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-05998	PCBA,MLB,3.2GHz,X1036,512G_TB,ENET_10G	COMM_BOM,CPU:3.2G,SSD:512_TB,X1036_ENET_10G,SOC:1G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-06006	PCBA,MLB,3.2GHz,X1036,1T_SD,ENET_10G	COMM_BOM,CPU:3.2G,SSD:1T_SD,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-06004	PCBA,MLB,3.2GHz,X1036,1T_TB,ENET_10G	COMM_BOM,CPU:3.2G,SSD:1T_TB,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM
	639-06010	PCBA,MLB,3.2GHz,X1036,2T_SM,ENET_10G	COMM_BOM,CPU:3.2G,SSD:2T_SM,X1036_ENET_10G,SOC:2G_DEV,ALTERNATE,DEV_BOM,10GDBG_BOM

3.6GHz 4C
ENET_1G

3.6GHz 4C
ENET_10G

2.8GHz 6C
ENET_1G

2.8GHz 6C
ENET_10G

3.0GHz 6C
ENET_1G

3.0GHz 6C
ENET_10G

3.2GHz 6C
ENET_1G

3.3GHz 6C
ENET_10G

Note:SSD SD and WD are the same

BOM_COST_GROUP=PCB

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

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Apple Inc.

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X1036 BOM Groups

BOM GROUP	BOM OPTIONS
X1036_COMMON_ALL	ALTERNATE,COMMON,X1036_COMMON1,X1036_COMMON2,X1036_COMMON3,X1036_DEFAULT
X1036_DEFAULT	SSD0_NAND_VCC:2.5V,ALL_SYS_PGD:1V8,SPIHOLD:H9M,CPUPEG:X8X4X4
X1036_COMMON1	X1036_PROGRAMMABLE:ENG,X1036_MODULE_PARTS:ENG,X1036_REV:DVT
X1036_COMMON2	X1036_HDMI,X1036_ID
X1036_COMMON3	LOADISNS,VR_BULKCAP:CURRENT,SENSOR:DEV,LOADRC:YES,ENGISNS:YES,XDP:YES
X1036_ENG:NO	FAN_DBG
X1036_ENG:YES	XDP_CONN,WIFI_DBG,USBC_DBG,SOC_DBG,SSD_DBG,LEDS_DBG,SOCMUX_DBG:YES,BUTTON_DBG
X1036_PROGRAMMABLE:ENG	TBT_T_ROM:DVT,TBT_X_ROM:DVT,BT_FLASH:DVT,WLAN_EEPROM:DVT,SOC_ROM:BLANK,SEPROM:OG,HDMI_ROM:DVT
X1036_MODULE_PARTS:ENG	PCH:PRQ,TBT_TR:C1,ACE:C0,PMU:A0_C,WIFI:ES7,HDMI:A4
X1036_HDMI	CLK_FILT,DATA_FILT,HDMI_RST:OD
X1036_ENET_10G	ENET:10G,10G_ENET:B1,10G_ENET_ROM:DVT,ENET_REFCLK:OSC
X1036_ENET_1G	ENET:1G,1G_ENET:A0,1G_ENET_ROM:DVT
X1036_ID	BOARDID1,BOARDID2,BOARDID3
X1036_REV:DVT	BOARDREV2,BOARDREV1,BOARDREV0
X1036_DEVEL:DVT	X1036_ENG:YES,ALTERNATE
X1036_DEV_1G_ENET	LED_1G_ENET_DBG,ALTERNATE
X1036_DEV_10G_ENET	DEBUG_LEDS:10G,ALTERNATE

COMMON BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00130	COMMON PARTS,MLB,X1036	X1036_COMMON_ALL

DEV BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
985-00836	DEV(DEBUG)_COMMON PARTS,MLB,X1036	X1036_DEVEL:DVT
985-00853	1G ENET DEV/DEBUG PARTS,MLB,X1036	X1036_DEV_1G_ENET
985-00854	10G ENET DEV/DEBUG PARTS,MLB,X1036	X1036_DEV_10G_ENET

BOM VARIATION

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
985-00836	1	COMMON DEV/DEBUG,MLB,X1036	DEVEL	CRITICAL	DEV_BOM
685-00130	1	COMMON PARTS,MLB,X1036	COMM	CRITICAL	COMM_BOM
985-00853	1	1G ENET DEBUG,MLB,X1036	1G_DEVEL		1GDBG_BOM
985-00854	1	10G ENET DEBUG,MLB,X1036	10G_DEVEL		10GDBG_BOM

Alternatives section 2

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S00042	128S0329	ALL	CB200 etc rdr 37042037	
128S0311	128S0329	ALL	CB200 etc rdr 37042037	
353S00107	353S3239	ALL	U5400 erc rdr 37173893	
353S1429	353S3239	ALL	U5540 erc rdr 37175030	
107S00055	107S00090	ALL	U5540 erc rdr 37175230	
107S00056	107S00086	ALL	R5430 erc rdr 37175329	
107S0276	107S00020	ALL	R5600 erc rdr 37175569	
103S0321	103S0276	ALL	R5545 erc rdr 38515379	
138S0775	138S0860	ALL	C3198 etc rdr 38305368	
138S00049	138S0831	ALL	C8611 etc rdr 38306891	
311S00192	311S00191	ALL	U8312 etc rdr 37077481	
138S00024	138S0986	ALL	C3701/2/3 rdr 37399555	
103S00248	103S00247	ALL	R9000 rdr 38514938	
103S00250	103S00249	ALL	R9001/3 rdr 38515246	
128S0364	128S00081	ALL	C6482/3 rdr 37292870	
128S0264	128S00081	ALL	C6482/3 rdr 37292870	
377S00103	377S00138	ALL	DZB801/2 rdr 36419223	
377S0124	377S00138	ALL	DZB801/2 rdr 36419223	
138S00013	138S0772	ALL	C9921 rdr 38080947	ENET:10G
118S00093	118S00092	ALL	RA720 etc rdr 38513679	
138S0945	138S0706	ALL	C6360 etc rdr 38310616	
155S0387	155S0694	ALL	LA601 etc rdr 39358850	
155S00204	155S0731	ALL	FLA800 etc rdr 39359536	
138S00084	138S00060	ALL	C2950 etc rdr 38312295	
371S00085	371S00190	ALL	D3100 etc rdr 39225721	
138S00262	138S0806	ALL	C6000 rdr 39360099	

BOM_COST_GROUP=PCB

SYNC_MASTER=Mary SYNC_DATE=04/26/2018

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